EDN

computer hardware In this Issue

exclusively for designers and design managers in electronics

EEE

aged Patient Safety

A CAHNERS PUBLICATION

OCTOBER 15, 1971

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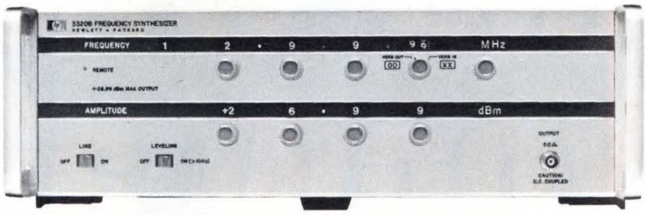
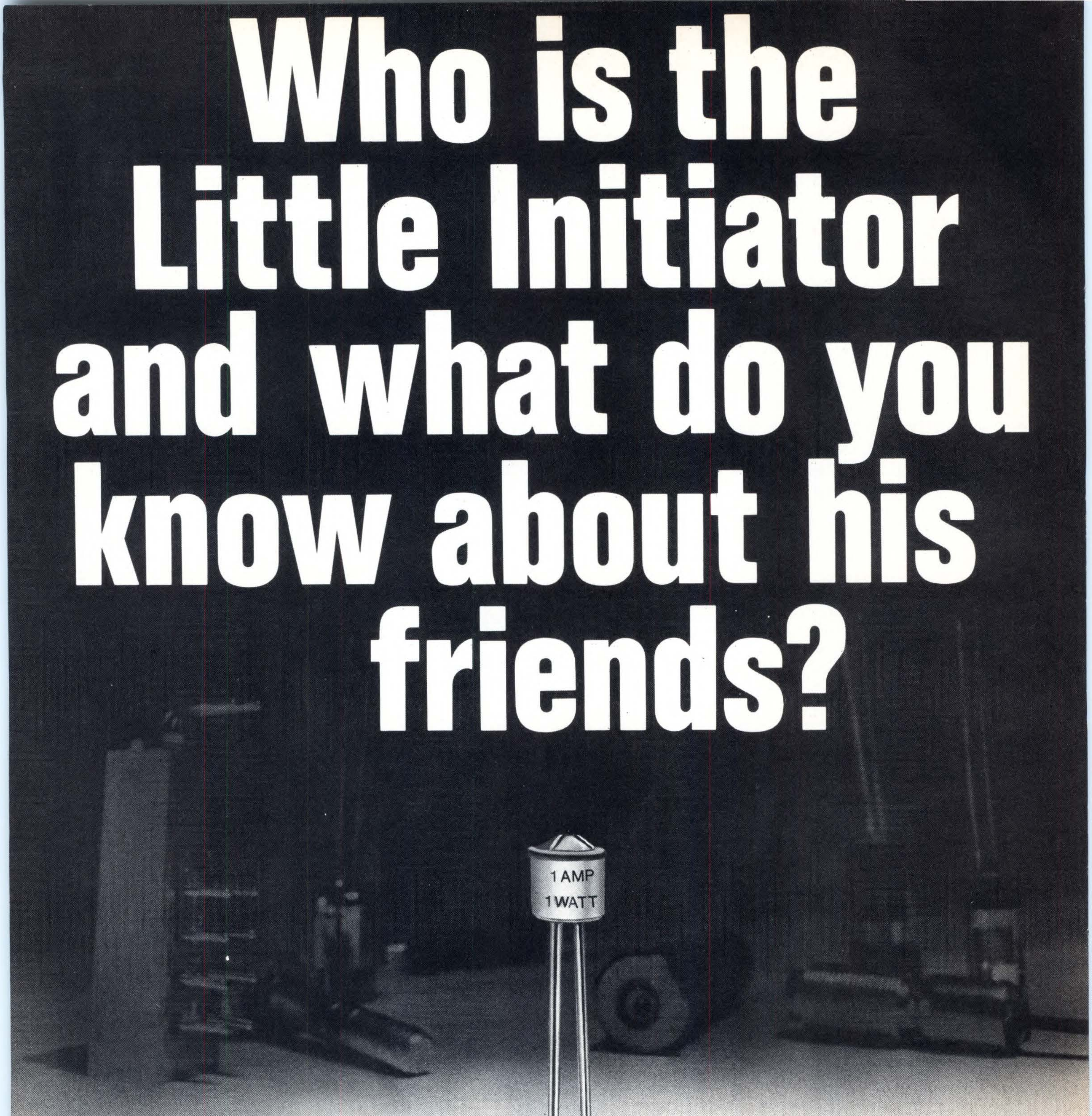


091/18

...at $1900, It's a Steal!

CIRCLE NO. 2



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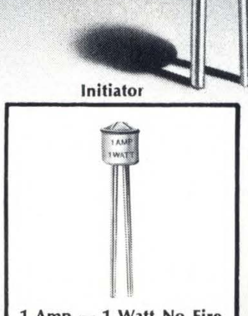

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CELANESE PLASTICS

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OCTOBER 15, 1971
VOLUME 16, NUMBER 20

EDN/EEE

EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

Cover

Cover photo by EDN/EEE's Art Director, Ray Lewis, shows a new medical isolation amplifier from Terradyn, Inc., along with a closeup of the optoelectronic coupler that is its heart. See news story on p. 12.

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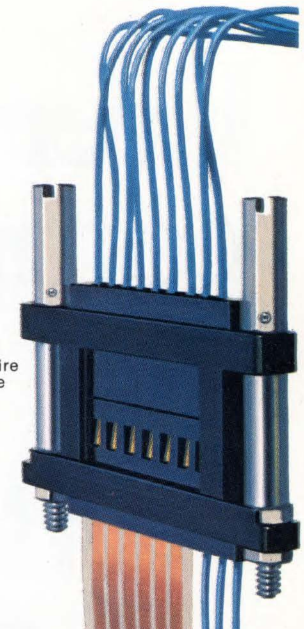

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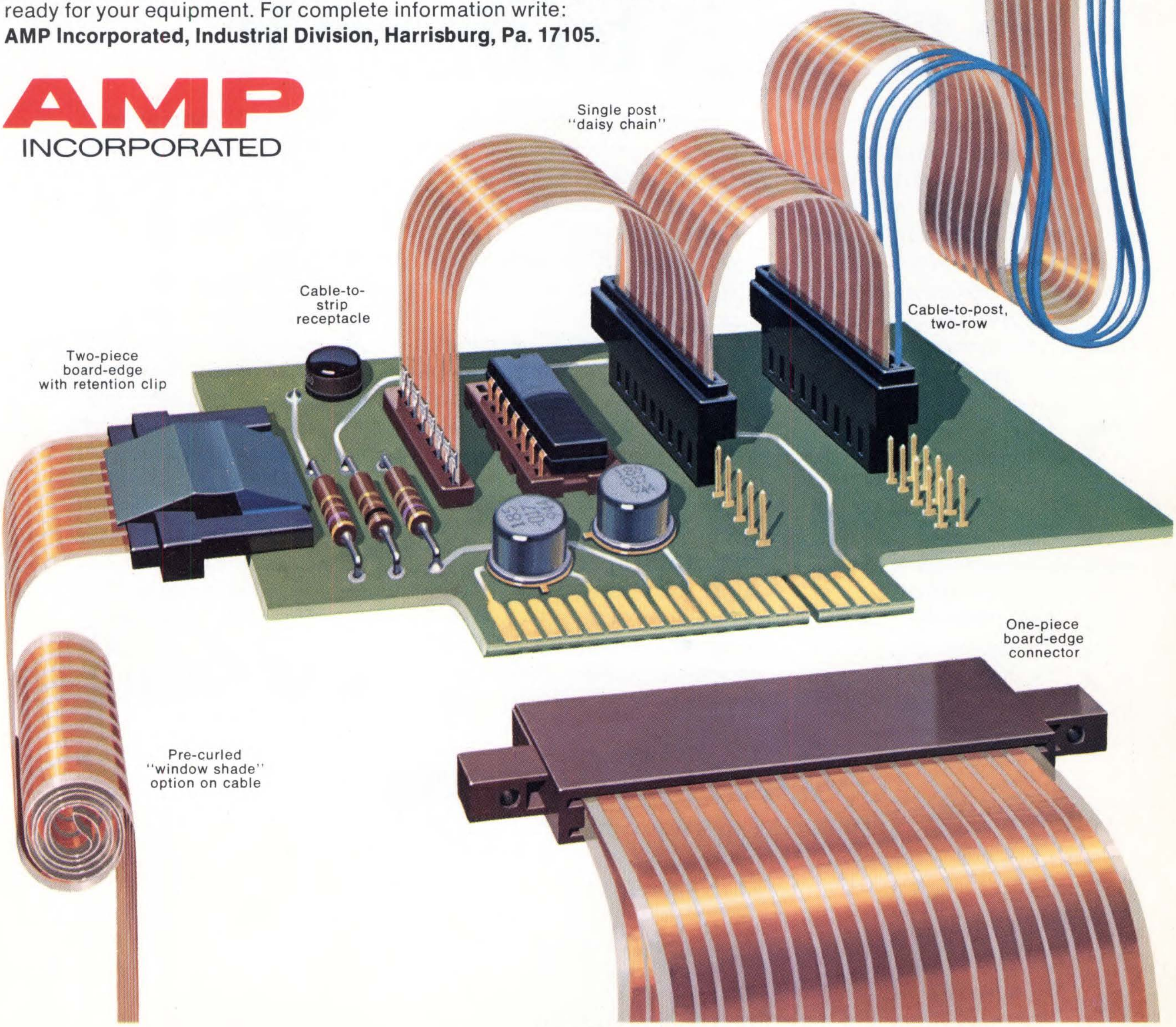

CIRCLE NO. 7

Editorial

Wages and Prices Aren't the Only Things That Can Be Frozen

President Nixon's wage and price freeze will be over soon and the full extent of its effectiveness in controlling inflation will be debated for some time to come.

The thought occurred to us recently that a similar freeze on specsmanship might be just what the doctor ordered for the electronics industry. In other words, for 90 days, or maybe 6 months, engineering efforts could not be aimed at what might be termed "spec stretching."

Development of the "fastest" analog switch, or the "smallest" thermal relay, or the potentiometer with the "lowest" temperature coefficient would have to wait. And instead, engineers would concentrate on improving things like the life, reliability and safety of existing products. They would also have considerable time to investigate ways to manufacture existing products cheaper, with the resultant savings passed on, hopefully, to users.

The benefits of such a freeze are obvious, particularly nowadays, when shifts in emphasis in the electronics industry have made things like price, life and safety more important than they ever were. This was brought home sharply at a recent trade show where the big crowds were at the booths featuring mundane selling points like price and delivery. Traffic at booths featuring products that were pushing the state-of-the-art, on the other hand, was generally light.

Some will argue that the very purpose or essence of engineering is technological progress—and that a freeze of this type would be counter to basic engineering goals. We wonder, though, whether these people are forgetting that technological progress must have a practical and useful purpose if it is to be meaningful.

All of these are moot points, of course, since no one is going to impose a freeze on engineers. A lot could be learned, though, by just thinking about the possibility.

Frank Egan

EDITOR

Staff

Most designers specifying copper for a component are satisfied to get through a single brazing run with no hydrogen embrittlement. That wasn't good enough for the assemblies in the new Los Alamos Scientific Laboratory 800 MeV linear proton accelerator. Many of them had to go into the furnace six different times. Without hydrogen embrittlement, without jeopardizing previously brazed joints, and without affecting conductivity.

In addition the parts were forged, extruded, or welded; and machined numerous times.

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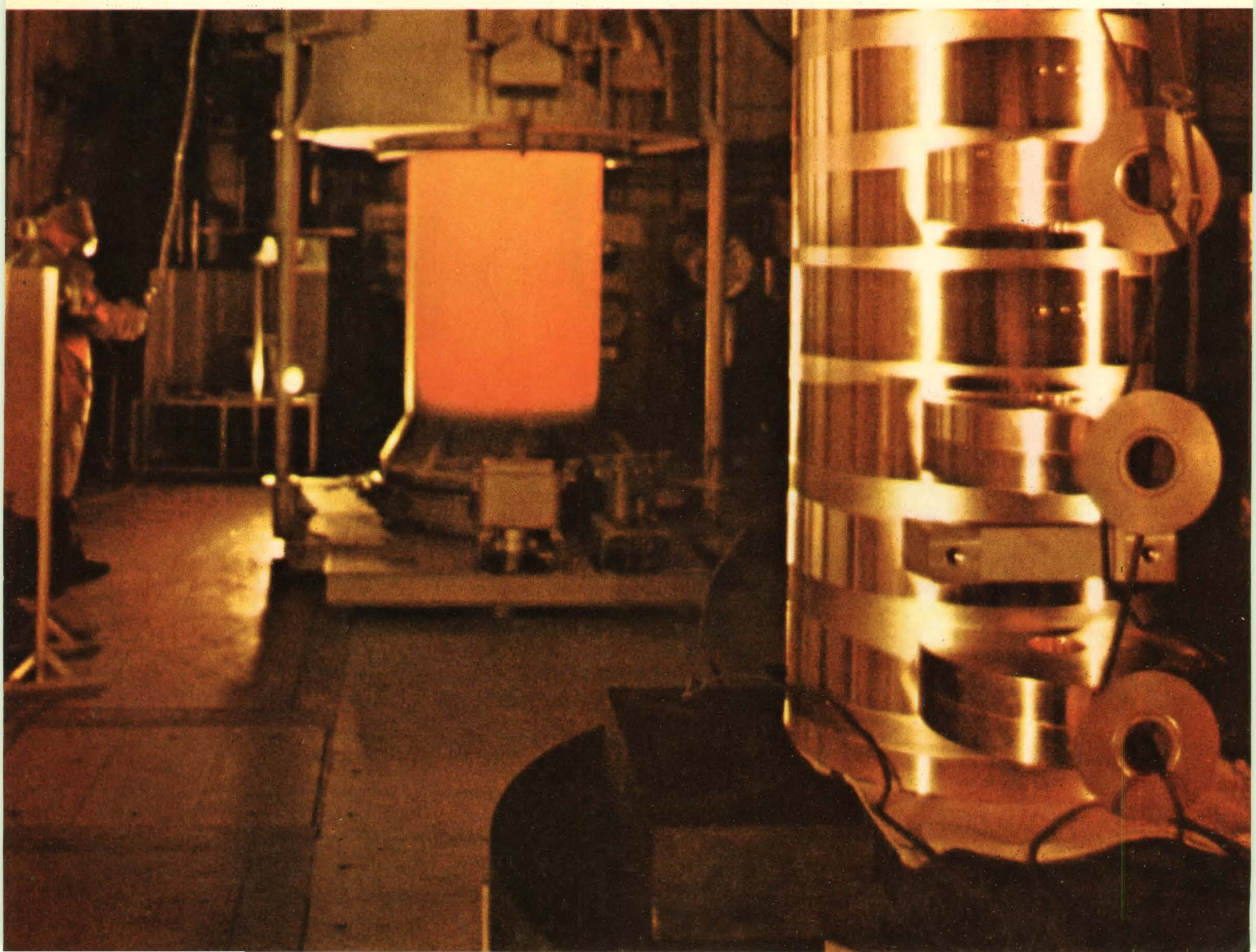
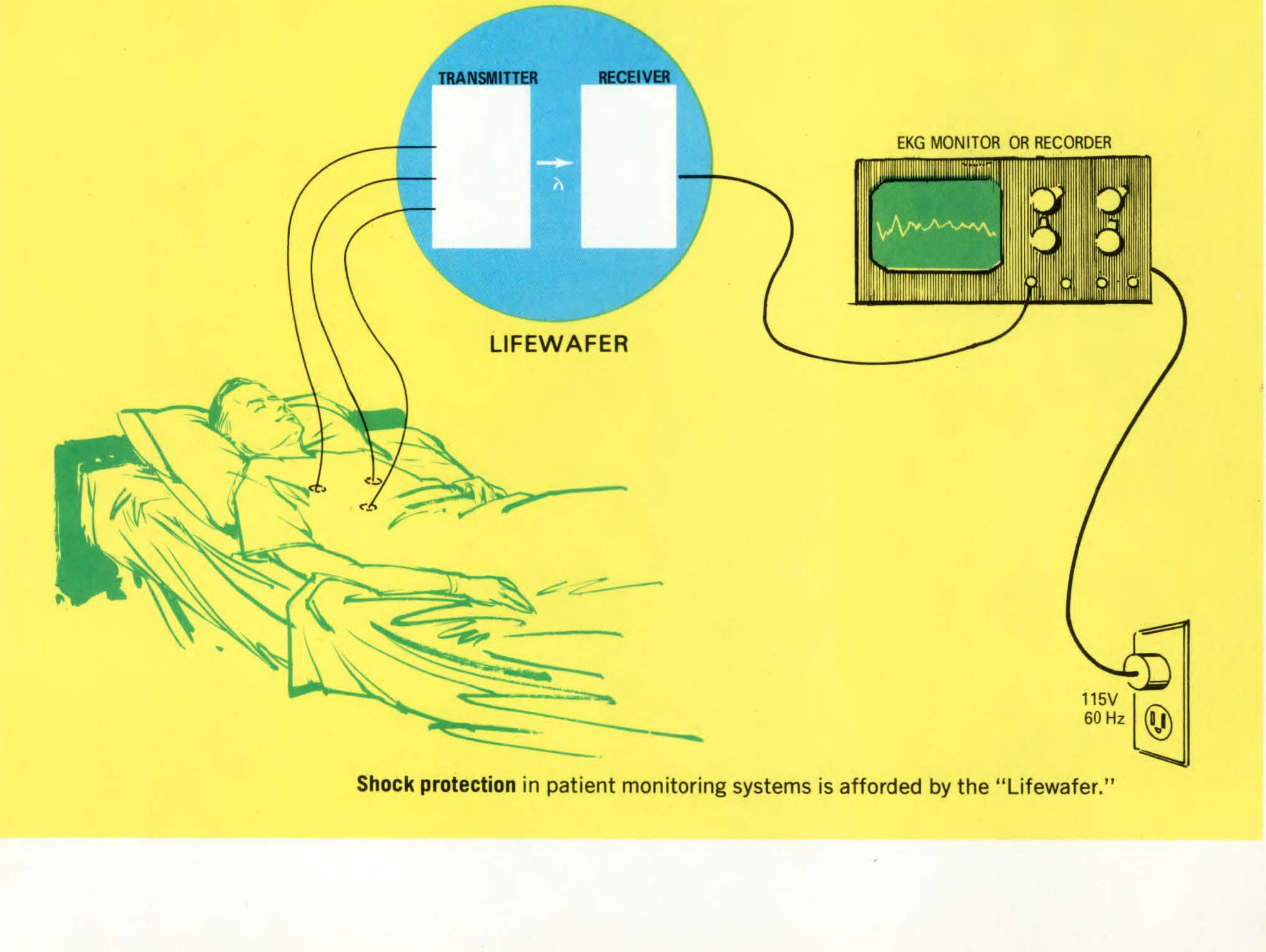


Optoelectronics and Micropower Halt Hospital Hazards

Hospital patients who now are instrumented to medical electronic equipment have gained a new friend. Terrasyn, Inc. of Longmont, Colorado has completed the design and evaluation of a new shock-preventing isolation amplifier for use with EKG monitors or chart recorders. Named "Lifewafer," it uses opto-electronic isolation and operates at very low power levels.

Circuit Design. Isolation is accomplished with a soon-to-be announced optoelectronic coupler (gallium-arsenide emitter, glass fiber optics and silicon sensor). Specs for this coupler include 10-kV isolation, dc resistance of $10^{14}\Omega$ and less than 0.3 pF of ac coupling.

By employing a voltage-controlled oscillator to pulse the gallium-arsenide emitter at 1% duty cycle, and by using some very careful circuit design, the dissipation of both transmitter and receiver portions of this amplifier was held to 150 μW. Output impedance is a low 5 kΩ. Such extremely low total power dissipation was necessary because a decision had been made in favor of throw-away batteries. Before selecting the throw-away type, comparison was made with rechargeable batteries, but the latter's cost and physical size precluded their use in this application. Also, since hospital personnel use this amplifier, both convenience and



Shock protection in patient monitoring systems is afforded by the "Lifewafer."

training were major design criteria.

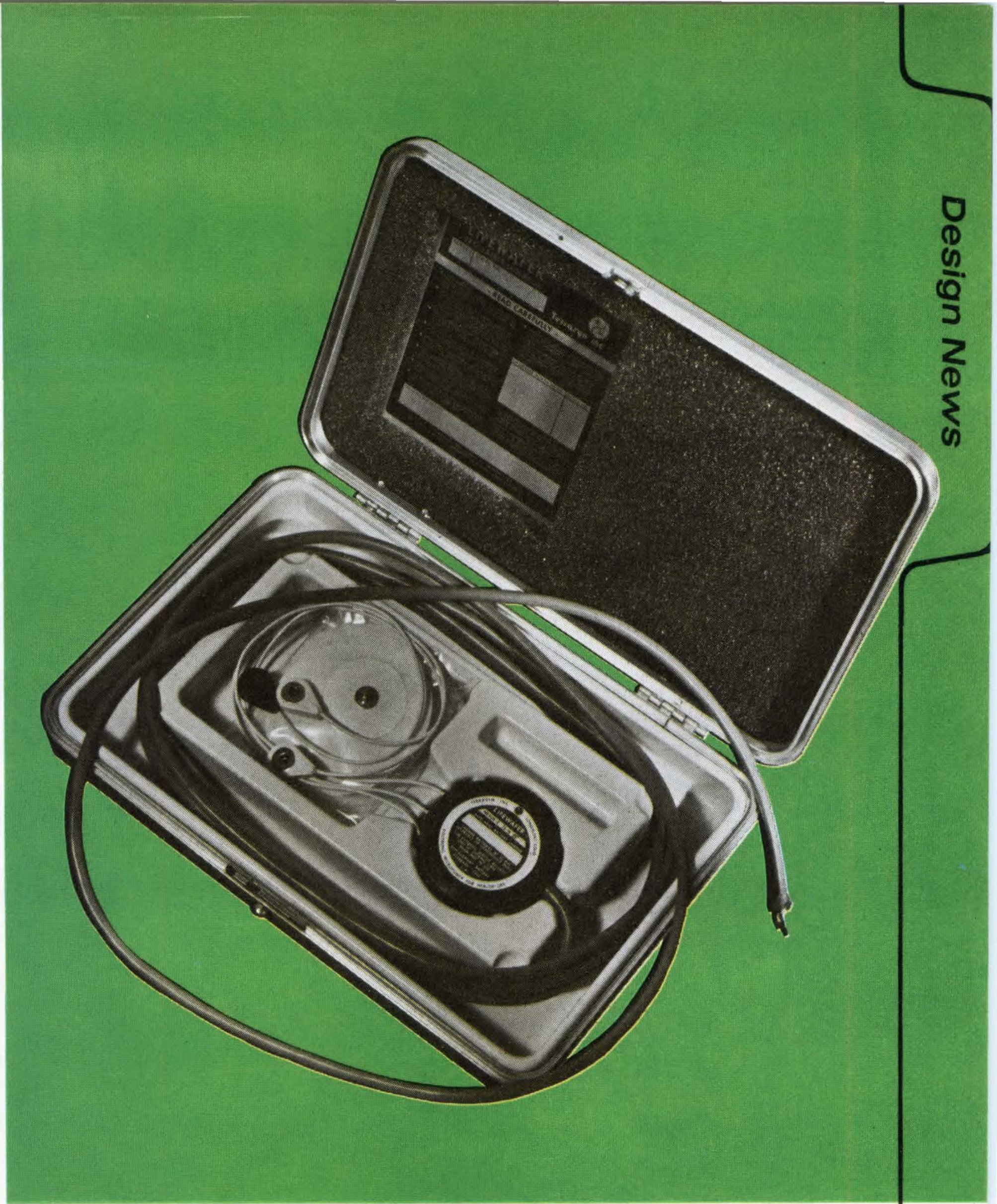
Much care was taken in the input circuit design. Because the normal 0.1- to 5-mV patient input signals to the amplifier occur in the presence of up to 200-mV offsets, the input circuitry must ignore these offsets. Also, input impedance must be high, yet the unit must function in a high-level 60-Hz noise environment.

In this device there is no reference to earth ground. Instead, differential signal inputs are referenced to their own return, resulting in a virtual common-mode rejection of better than 100 dB. This provides adequate rejection of 60-Hz pickup while achieving 100-MΩ input impedance in each leg to insure that maximum patient current will be kept well below 10 μA.

When operated near such items as electric razors, drills or microwave ovens, this amplifier is completely insensitive to stray pickup. Also, the input circuitry will withstand, with no damage to the internal electronics, a 7-kV defibrillator discharge on any combination of input leads.

Packaging Design. It is commonly agreed that for maximum patient safety, current limiting should be done as near to the patient site as possible. This new amplifier comes ready to meet this need with no user training required.

For three reasons—to permit a sealed case, to avoid any need to instruct the user to turn the unit on and to keep the patient from having any control over the amplifier—biased reed switches are used to connect the batteries to the circuit. When the unit is in its carrying case, these switches are biased open by magnets mounted inside the case. When the amplifier is removed from the case, the internal reed switches close and the unit starts to operate.

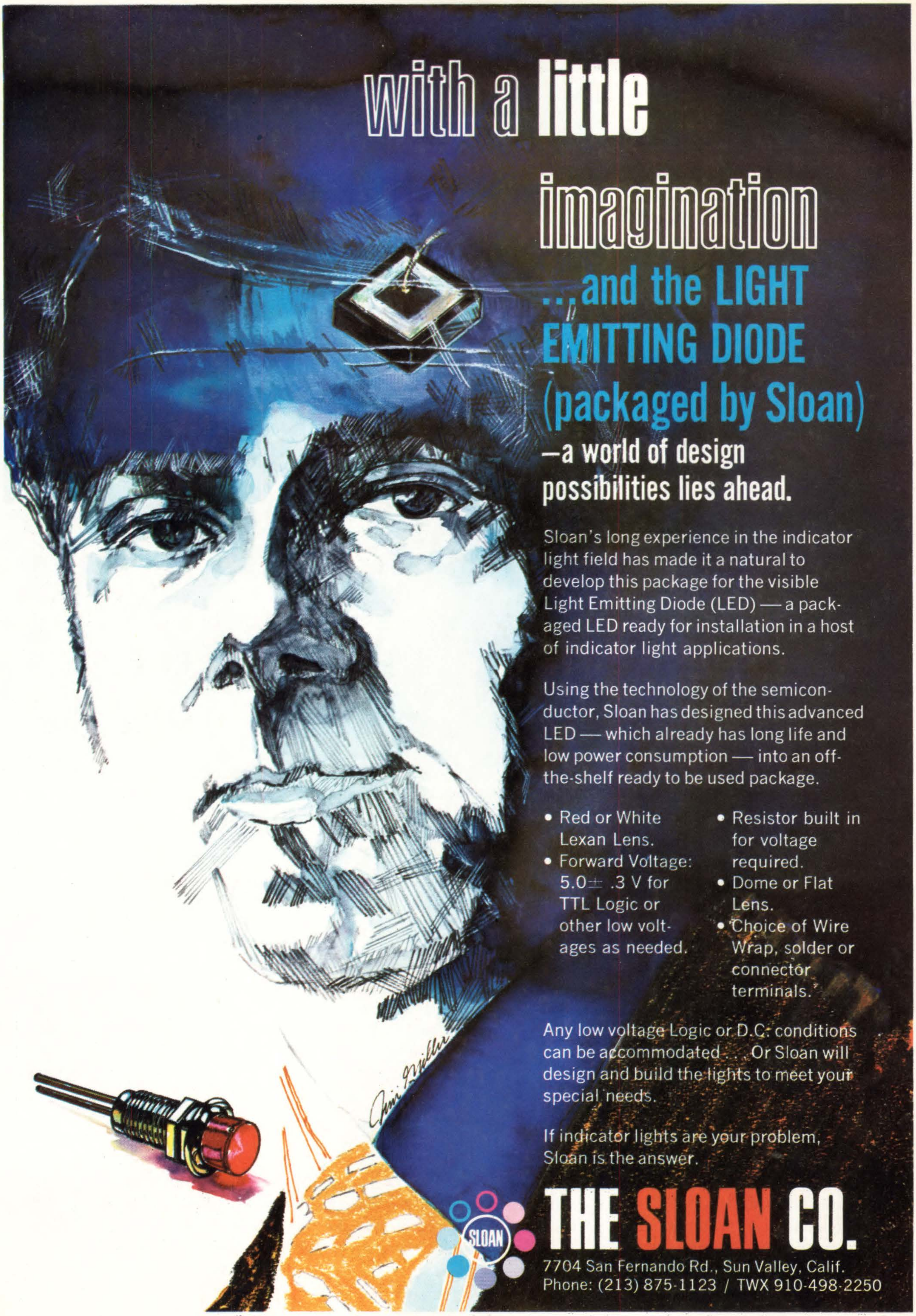


The "Lifewafer" is connected to its battery power by biased reed switches which are controlled by magnets mounted inside the case. The reed switches close to energize the unit only when it is removed from the case.

Double duty is performed by the "Lifewafer." It can replace, directly, the cable that now connects from a patient to a bedside monitoring system. When used this way, outputs are floated with respect to system monitor ground. In its other application it performs as a single-ended output amplifier, raising the millivolt patient signals for sending over long lines to a remote EKG monitoring system. Used either way, it provides complete isolation for the patient. The package has no sharp corners or edges that could cause injury. Also, the GE "LEXAN" plastic used for the case is impervious to acids and other external body fluids, contains no toxic dyes and is easily sterilized.

Inside the unit, the PC module is sealed against moisture, and there is no metal on the package surface. Even the printing is done with a dielectric ink to insure against conductive paths.

This amplifier will update yesterday's equipment to meet the stringent demands being imposed today. To put it to use, all that is required is to remove it from the case, plug it in to replace the old cable and mark the battery change date on the case.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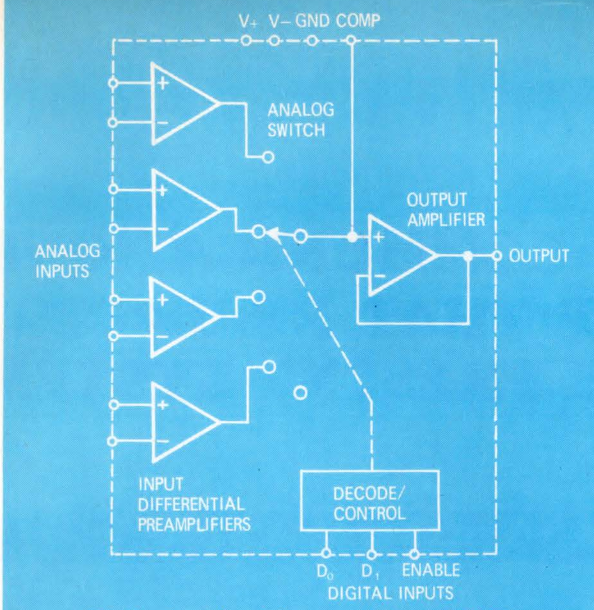


Fig. 1—**Functional diagram** of the HA-2400.

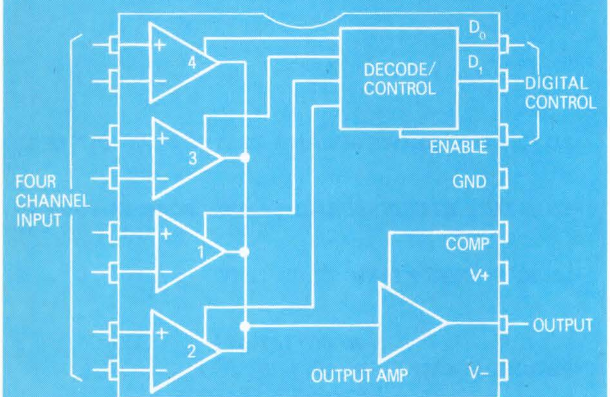
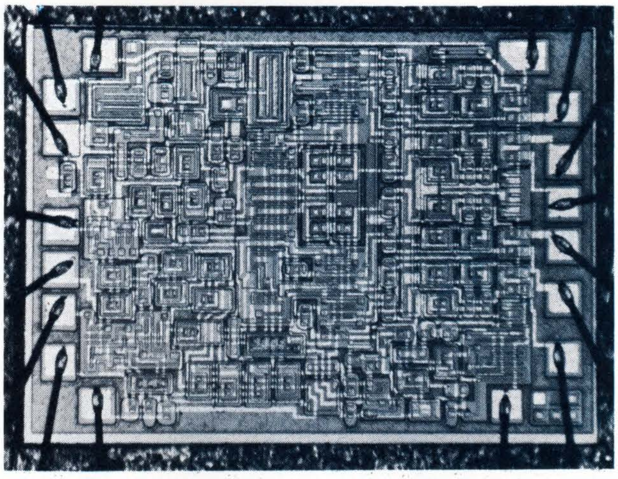


Fig. 2—**Circuit block diagram.**

Programmable Analog Module Provides Design Versatility



IC contains 4 input preamps, an output amplifier and decode/control circuitry in 16-lead hermetically-sealed DIP.

D_0	D_1	ENABLE	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4
L	L	H	ON	OFF	OFF	OFF
H	L	H	OFF	ON	OFF	OFF
L	H	H	OFF	OFF	ON	OFF
H	H	H	OFF	OFF	OFF	ON
L or H	L or H	L	OFF	OFF	OFF	OFF

$0V \leq L \leq +0.8V$ $+2V \leq H \leq +5V$

Table I—**Digital input truth table.**

"Instrument on a chip" is a step closer to reality with a new concept in ICs introduced by Harris Semiconductor. Actually, instruments (plural) would be more accurate because this DIP building block (called the HA-2400 PRAM) can be used to construct a variety of circuits. The significance of this development is not in the complexity or in the amount of circuitry packaged on a chip, but in the versatility provided by the packaging concept and design.

Consider what you might do with a package consisting of four input preamplifiers, an output amplifier and a means of digitally connecting one of the four input amplifiers to the output amplifier (**Fig. 1**). Actually you can do anything you could with a conventional op amp. Then throw in the advantage of programmability, and you can do much more.

For example, by connecting similar feedback networks from the output to each of the four input channels, the device can select and condition several input signals. Conversely, by connecting different feedback networks to each of the inputs, various op amp functions can be performed on a single input signal.

Although programmability is a key feature, it does not necessarily have to be utilized. The PRAM can be used with one channel as a high-performance op amp.

A Look Inside. The actual circuit (**Fig. 2**) consists of four preamps whose outputs are connected in parallel to the output amplifier. Operating current is furnished only to the selected input channel by the decode/control circuitry, thus switching that channel to the output amplifier. Input terminals of the OFF channels are effectively open circuits.

Digital inputs, D_0, D_1 and enable, control the input channel selection according to the truth table (**Table I**). These inputs can be driven with any DTL or TTL circuit that uses a standard 5V supply.

Frequency compensation for closed-loop stability is recommended when closed-loop gains are less than 10. A single external capacitor across two pins does the job. When different feedback networks are used, the channel with the lowest closed-loop gain governs compensation requirements.

Putting It To Use. Obviously, the PRAM is not just another integrated-circuit op amp with improved specifications. It is a building block that should provide economical solutions to designers' problems and perhaps stimulate the development of improved products.

A few applications suggested by the manufacturer include: programmable gain amplifier (inverting or noninverting), programmable adder/subtracter, phase detector and track-and-hold/sample-and-hold—to mention just a few. Design engineers, ingenious as they are, will undoubtedly find a host of other jobs for the PRAM to do.

For further information, contact Harris Semiconductor, Box 883, Melbourne, FL 32901.

Retraining Studies Employ Aerospace Engineers

Two federally-assisted programs are under way to find methods for aerospace and defense technical personnel to apply their experience in solving today's social and ecological problems.

Both programs use unemployed engineers and scientists to do the work, but their emphases are slightly different.

In Atlanta, Georgia, the combined efforts of the citizens of Cobb County, Emory University and the National Science Foundation have resulted in employment of 21 people in the Partners for the Advancement of Cobb Economy (PACE) Corporation. They will determine research needs in areas such as waste disposal, health care, transportation and water pollution, and then design research projects aimed at solving problems in these areas.

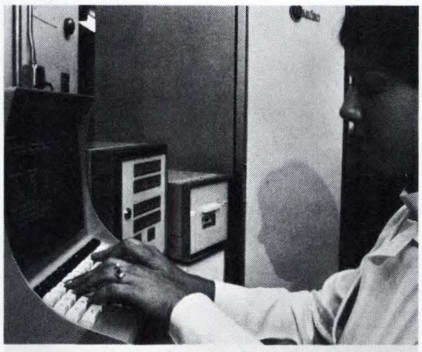
Projects will be reviewed by a committee to select appropriate ones for further development either by Emory University or by PACE. The study program will provide a certain amount of retraining by placing unemployed technologists in a new kind of problem solving situation.

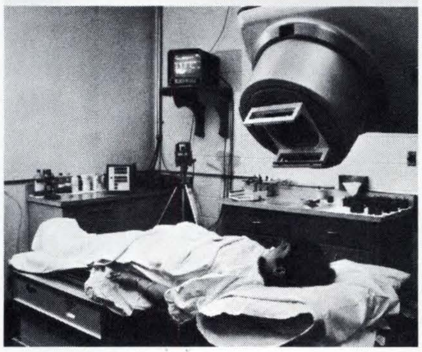
The other program, involving the NSPE and six other professional engineering societies, is funded by the Department of Labor. Study teams will be set up in Seattle and Los Angeles initially, with teams to follow in 12 other areas of high professional unemployment. These teams will be assigned specific industries for study with the following objectives:

1. Identify skills needed in the near future in specific fields.
2. Identify specific skills of unemployed professionals that can be used to fill the need.
3. Create a base of information identifying skills that are transferable, under what conditions and to which alternate occupations.
4. Develop a mechanism for effecting the conversion, including training, reorientation and job identification.

These programs recognize the need for the unemployed engineer or scientist to make a living during his retraining phase, and to be retrained in an area where there is actually a need and employment opportunity. Both are examples of the type of realistic thinking needed to solve the problems of the engineer today.

Minicomputer Controls Radiotherapy Treatment





A minicomputer-controlled radiotherapy system is now treating patients on a day-to-day basis with a 20-30% reduction in setup time at University of Wisconsin hospitals.

The new system, called CART (Computer-Assisted Radiation Therapy), consists of a Varian 620/i minicomputer and a Varian "Clinac" 4 linear accelerator in a single hardware/software package.

Increased efficiency in the treatment of patients on a day-to-day basis is possible because dosage prescriptions and treatment regimens are preserved on a single personalized 1/8-inch tape cassette. Each cassette contains information that provides automatic regulation of the 4 MeV Clinac's beam size, direction, patient couch position and other important treatment parameters.

Faster and more efficient handling of records and other medical administrative data is provided by immediate printout of each patient's treatment history from cassettes.

Valuable safety features, such as a collision-avoidance system and a redundant identification check before treatment, are provided to insure that the proper cassette is regulating the proper patient's treatment. In addition, the system verifies automatically that the treatment setup is as the therapist prescribed. Daily therapy patient load can be significantly increased without an increase in cost.

After placing a patient's cassette in CART's cassette reader, the technician enters the patient's identification number on the control room display. If the I.D. number matches that on the tape, the complete patient record is entered into the minicomputer. The minicomputer then proceeds automatically to the next step, which is a visual display of the accumulated monitor dose for each portal, the total accumulated monitor dose, the total number of treatments in the plan, the number given already and the next portal number to be executed.

The computer then compares prescribed treatment parameters with actual settings of the Clinac 4 and its control console and indicates discrepancies on the video monitor. The information which the minicomputer has received from the cassette is then used to control gantry position, beam size, couch position and size and angulation of the beam. When the computer determines that the setup criteria have been met, an appropriate ready light is turned on. This tells the X-ray technician that he may now turn on the beam. When treatment is finished, the "Teletype" automatically prints out the treatment parameters.

Besides substantial reduction of the possibility of human error, one of the chief advantages of the CART system is the ability to gather a good data base for retrospective studies at periodic intervals to upgrade treatment modes. For further information write to Dr. Richard Levy, Radiation Div., Varian Associates, 611 Hansen Way, Palo Alto, CA 94303.

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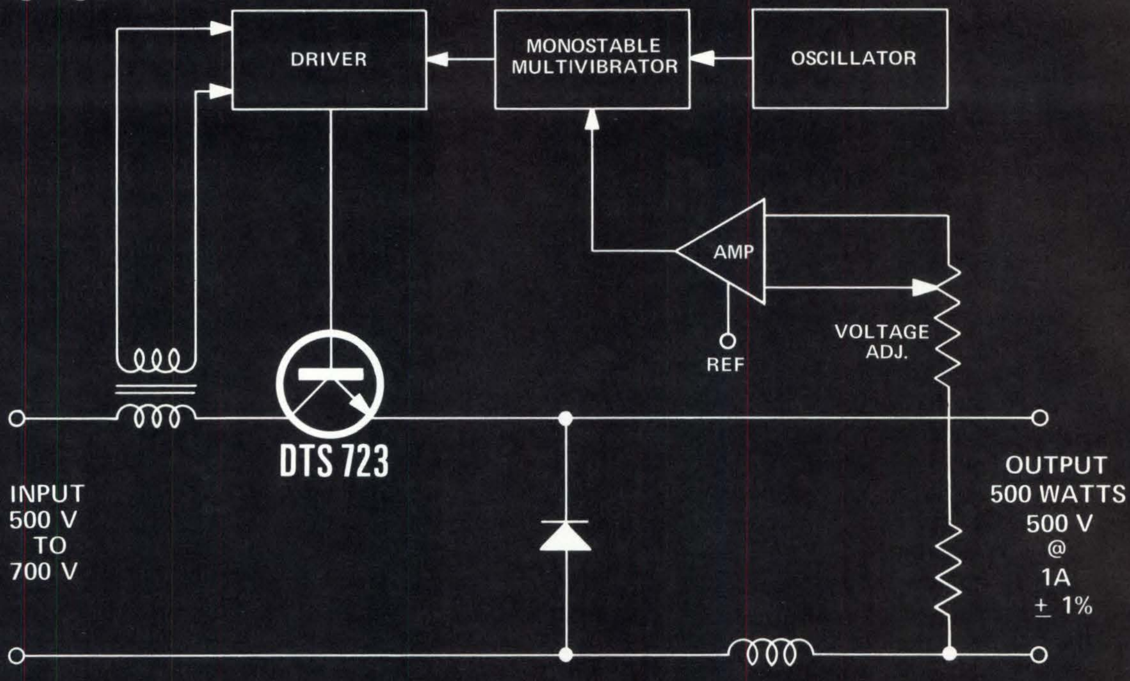
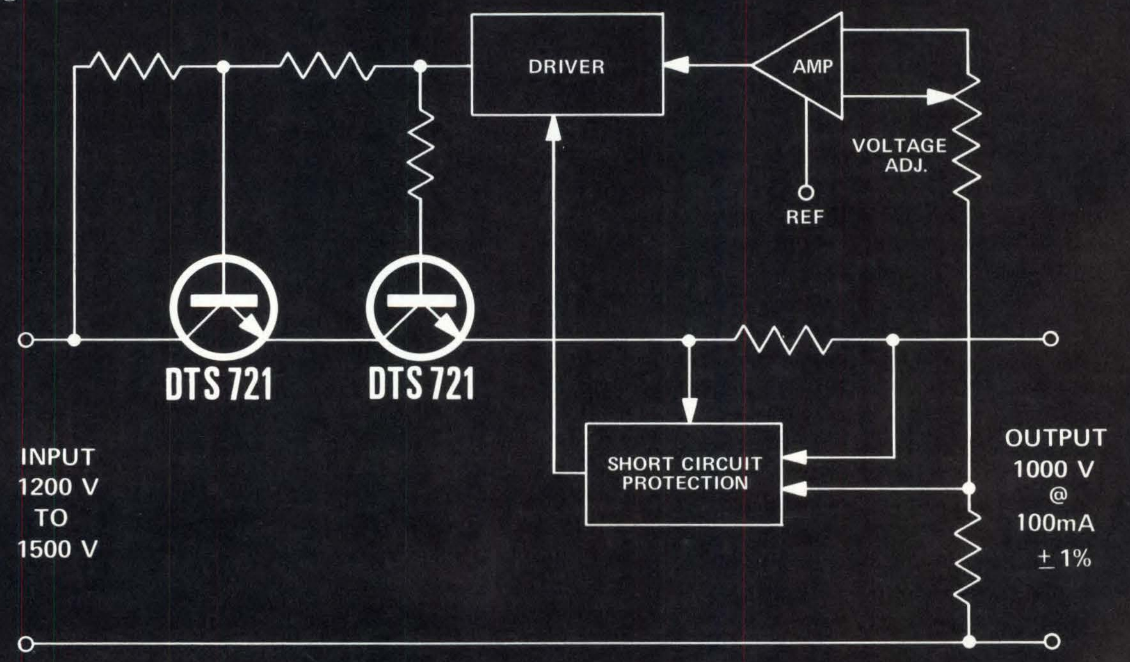
Switching Regulator



DC Regulator



	V_{CEX}	V_{CEO}	V_{CEO} (sus)	I_C (cont)	h_{FE} @I_C min/max V_{CE}=5.0V	P_T
DTS-721	1000V	1000V	800	3A	20/60 @ 150 mA	50W
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CIRCLE NO. 11

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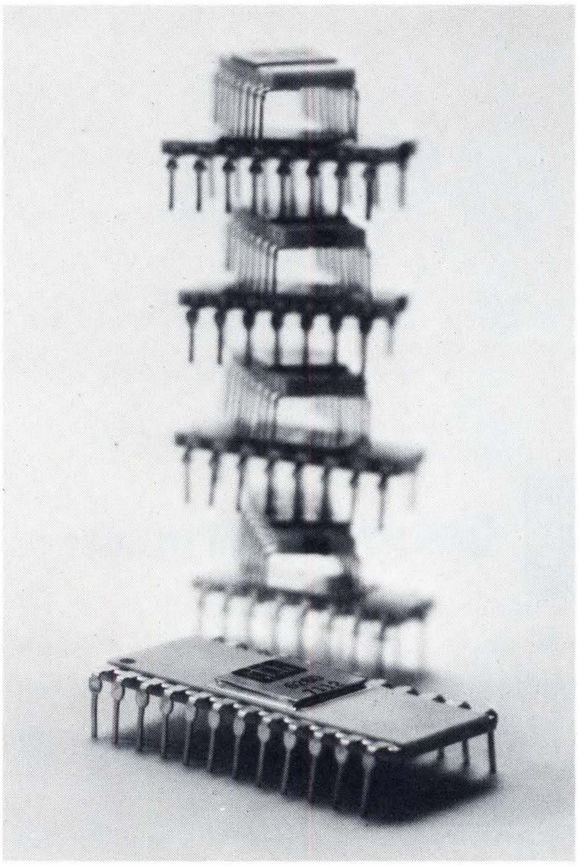
Introducing the world's first 8K bit bipolar read only memory.



Sooner or later someone was bound to do good things with bipolar memories. We did it sooner. Think about it. That's a lot of memory on one little chip. Even MOS can't touch it. With our new MM6280 you can replace eight 1K ROMs or 32, 256 Bit ROMs. Quite a savings when you consider one masking charge vs. eight, reduced P.C. card area, fewer interconnections, lower power requirement, lower insertion costs, and so on and so on.

On top of all that, it's got 100 nsec access time and nibbles only 60 microwatts per bit of power. It has four enable lines so you can go to 16K words without adding additional decoding. And no clocks are required because it is static.

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A few detail specs:

- 1024 words by 8 bit
- 60 microwatts per bit
- 100 nsec access time
- 4 enable lines
- 160 microamps address input current
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- Fantastic price: .7¢/bit in hundred quantity

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CIRCLE NO. 12

CONTROL MOS/LSI YIELD BY DESIGN

To gain an edge in today's competitive marketplace, many firms are converting their system designs into MOS/LSI. Consequently, today's designer must understand MOS/LSI yields as well as he does Ohm's Law. Equipment manufacturers must go a step further—they must develop an understanding of topological designs within their engineering ranks.

MEL PHELPS, Nortec Electronics Corp.

During the '60s, the electronic equipment designer had to relegate the entire process of semiconductor design and production to the semiconductor manufacturer. Typically this manufacturer ran the show. He decided what components to design and what risks to take, and customers who wanted more participation were forced to the sidelines.

MOS technology, with its 2-D design simplicity and relative standardization of processes, has changed all that. With MOS, performance is proportional to source-to-drain widths and lengths. No longer is there an air of mystery surrounding topology and layout. This has enabled equipment manufacturers to become actually engaged in the design process.

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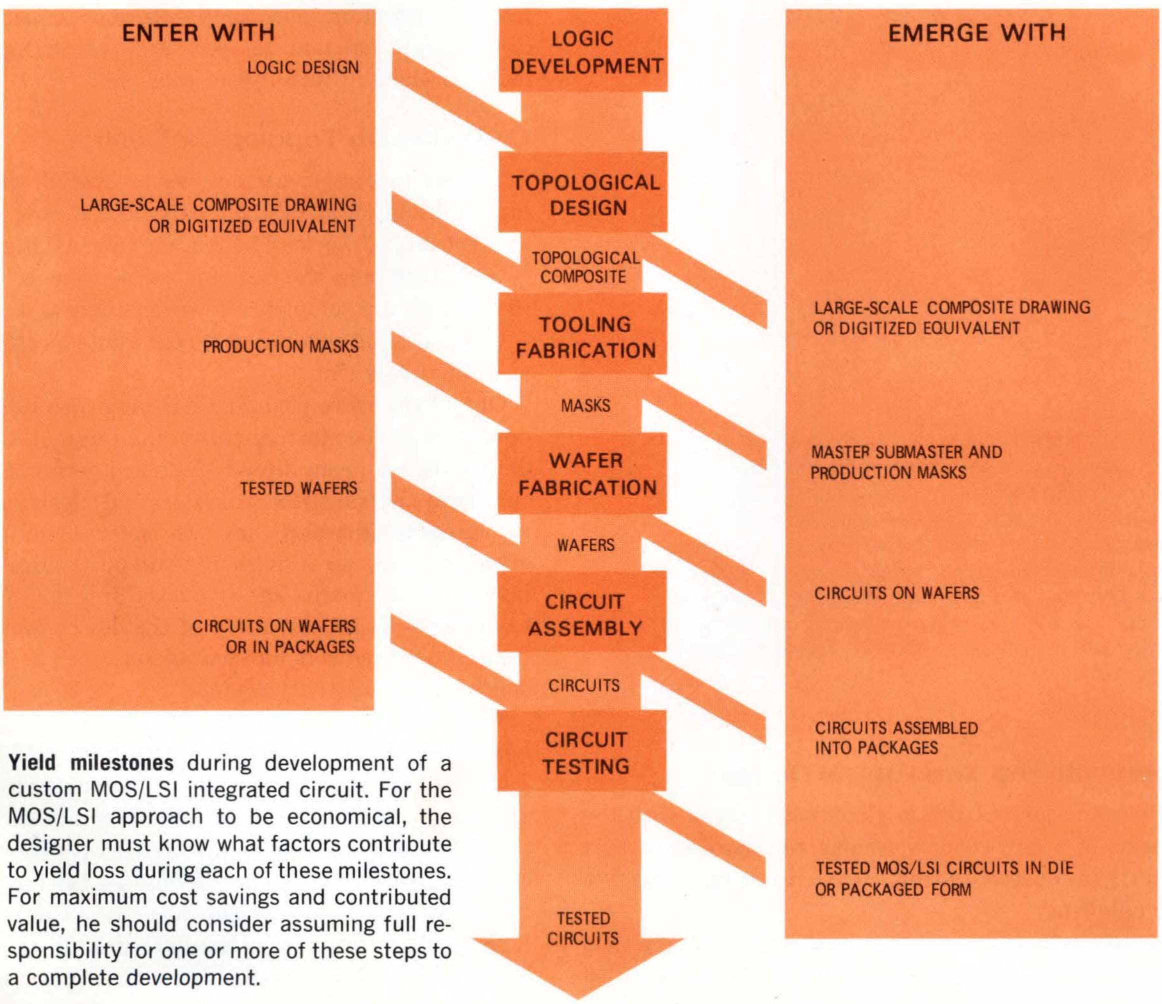

Yield milestones during development of a custom MOS/LSI integrated circuit. For the MOS/LSI approach to be economical, the designer must know what factors contribute to yield loss during each of these milestones. For maximum cost savings and contributed value, he should consider assuming full responsibility for one or more of these steps to a complete development.

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MOS/LSI Yield (Cont'd)

Designers accustomed to printed-circuit board topology are now turning directly to silicon as the interconnecting substrate instead of using glass-epoxy laminants surmounted by standard IC packages. As these designers swing to MOS/LSI, they must become much more knowledgeable about yields. This article will explore the factors that determine these yields and will detail how to maximize them.

'Think Yields' at the Outset

When we speak of integrated circuit yields, we are referring to the percentage of good devices that emerge from process, assembly and testing steps. Naturally, it is desirable to maximize yields at every one of these steps, because as the final yield goes up the cost per device goes down. As we shall see, several variables affect the final yield of an IC. Each of these variables must be optimized if maximum yield and minimum cost per device are to be achieved.

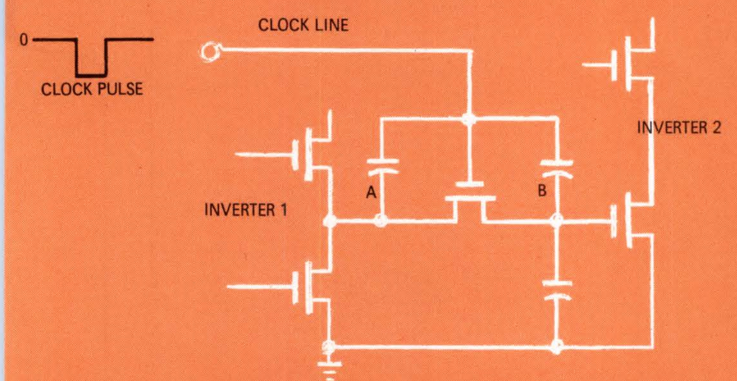


Fig. 1—**Improper design** always causes low yield. If the capacitive voltage divider for the MOS clocked inverters is not designed properly from a topological standpoint, marginal performance will result. For example, when the clock line goes negative, a negative charge is added to nodes A and B; when the clock line goes positive, a positive charge is added. As clock amplitudes vary, the added or subtracted charge can cause the logical "1" values to become marginal.

Start with the Topological Design

Planning for maximum yields must begin with the genesis of a circuit idea. Among the more important criteria to consider during the circuit design stage are the following:

Provide adequate noise margins for the expected range of process parameters. This can be achieved by insuring that inverter ratios are sufficient, that ground lines are solid and that gates and inverters are capable of driving their loads at the correct speeds.

Design capacitive voltage dividers properly. In dynamic MOS logic, capacitive voltage dividers are always present. If these dividers aren't properly designed, the noise margins will be inadequate and the circuit will not function as it should. This anomaly is detailed in **Fig. 1**. There are several ways to cope with this problem. One is to add extra capacitance to the divider network. A simpler solution, however, might be to use the vendor's standard cells, providing that they meet your design requirements.

Avoid NAND gates with more than four inputs. The active gate area is directly proportional to the number of gate inputs squared. Consequently, each additional gate input contributes substantially toward increasing the chip area—and the bigger the chip, the fewer the potential circuits and the lower the overall yield (see **Fig. 2**).

Use dynamic instead of static logic to minimize power dissipation and keep junction temperatures down. High junction temperatures cause increased leakage which in turn causes poor yield.

CAD Can Do Topological Design

Thanks to computer-aided design (CAD), the topological design of an IC need only take a few hours instead of several weeks. The accuracy of CAD is generally very good once the program conversions to the XY coordinates are complete. However, there is a tradeoff—CAD does not use the chip real estate as efficiently as a manual layout.

One of the more popular CAD programs uses standard cells as the starting point in the design. By standard cells, we mean already-designed geometrical circuit arrays of transistors, resistors and capacitors. This standard-cell approach has two major advantages: it gives the designer a quick reading on the topological layout of his circuit, and it allows him to ignore the basic physics and chemistry of the device fabrication (i.e., he need not compute parameters such as junction depth, sheet resistivities, etc.).

When using the standard-cell approach, the designer has access to hundreds of cells within the cell library. Typically, the cell library will accommodate any of the designer's electrical or functional requirements. By calling up the coordinates associated with the desired cell, the designer can immediately see his topological layout via a computer-driven plotter or a CRT display. If the proper circuit is not available within the cell library, it's easy to have the computer program provide a window in the program whereby the designer can

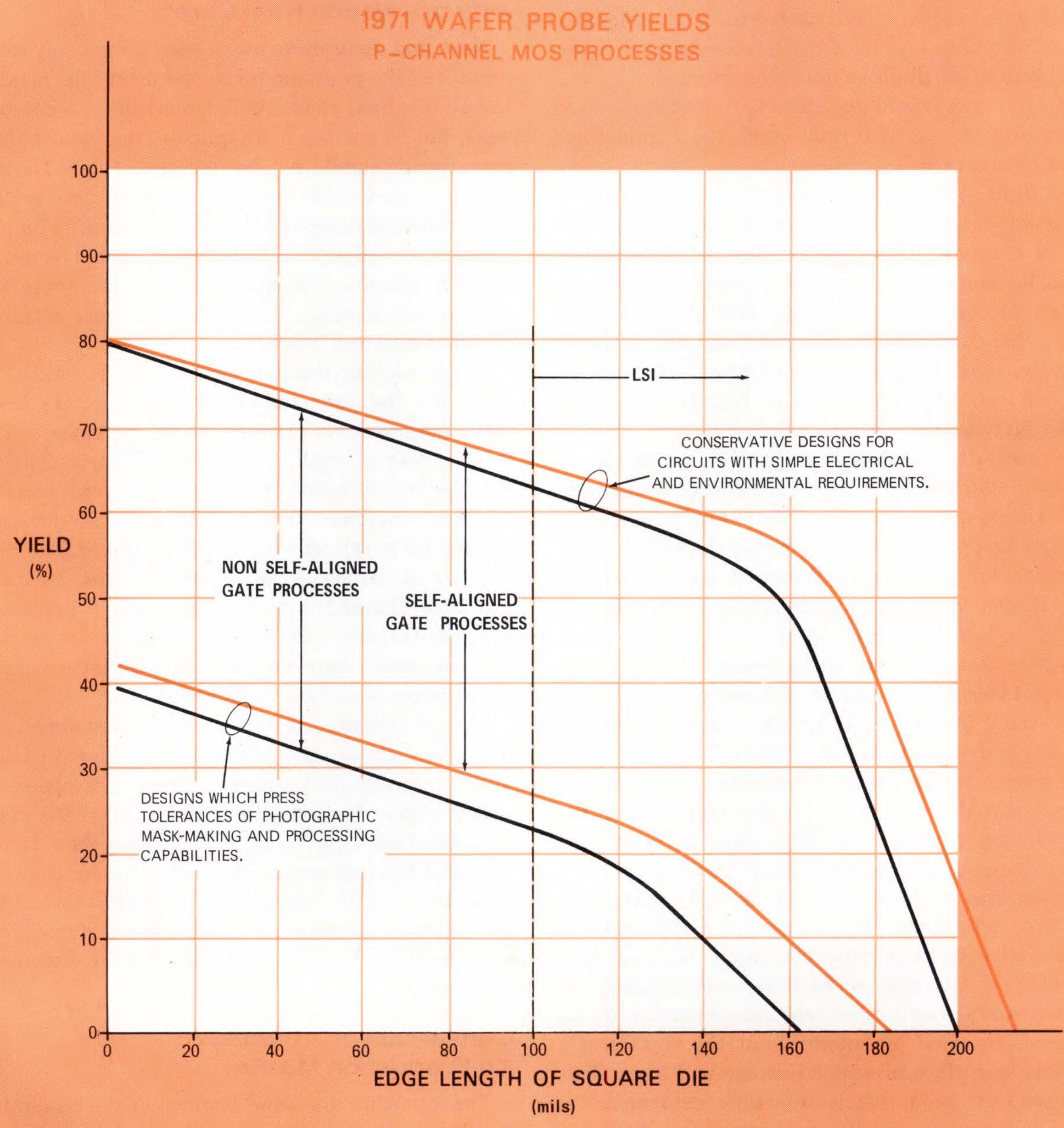


Fig. 2—**Chip size vs yield** is shown for both a loosely-packed and a densely-packed complex MOS circuit. Maximum yields are 80% and 40%, respectively. Yield drops off sharply for the loosely-packed device at about 160 mil^2—whereas the yield for the tightly-packed device drops off at approximately 120 mil^2.

(Continued)

add the necessary customized circuit. Aside from providing a fairly comprehensive cell library, such a CAD program also contains routing and folding instructions that describe how to interconnect outputs, inputs, power supplies and grounds.

Once a simulation or transient analysis is performed on a CAD topological design, the designer may want to go back and do some circuit customizing. Customizing to minimize chip area is always recommended if the circuit is to go into high-volume production.

If an IC's topological design is to contribute toward maximizing the device's final yield, these guidelines should be observed:

Avoid tight spots. In an attempt to maximize use of chip area, a designer is inclined to squeeze together parts of a circuit. This practice often leads to failure caused by aluminum breakage or shorts, p-p shorts, severe oxide steps, etc. Preventing such failures is easy if the vendor's design recommendations are followed. Typically, these recommendations provide for human error and tooling tolerances and are not as conservative as they may appear.

Avoid pinholes. Mask defects give rise to pinholes in the oxide which in turn cause p-p shorts, metal-substrate shorts and oxide ruptures. Pinholes are often traced to dust particles present during the photography performed for the mask-making or actual masking steps. Higher yields in large chip sizes are largely attributed to improved mask quality and to care taken during the masking steps of the process.

Reduce lateral pnp action. If a junction is forward biased, the substrate will clamp the p-region voltage at 0.7V above the substrate voltage by emitting minority carriers into the substrate. These carriers can then be diffused through the substrate and collected by the reverse-biased junction. And in dynamic MOS circuits, this can cause discharge of the data-storage capacitors. Following the vendor's design rules will usually prevent this lateral pnp action. However, the designer should strive to keep critical junctions isolated from any other junction that can be driven into forward bias.

Reduce surface inversion leakage. When the silicon surface is inverted by potentials at the surface of a thick oxide, surface inversion leakage will occur. This effect connects two p-regions from different transistors with a conductive path. Two ways to reduce this leakage are: 1) keep critical junctions away from high-voltage runs, and 2) isolate high-voltage runs such as V_{GG} supply with a diffusion connected to a lower potential (for example, lay out a diffused ground line between the V_{GG} supply and the rest of the circuit).

Minimize reach-through. When two adjacent diffusions get too close together, the depletion region from one reaches over into the depletion region of the other. Consequently, unwanted conduction occurs between the two regions. To minimize this "reach-through," the p-p material spacing should never be less than that recommended by the vendor.

Artwork Needs Real Care

Neat and accurate artwork goes a long way toward producing the precision masks necessary for maximizing an IC's final yield. Though machine-generated artwork can be created more quickly, the value of hand-cut artwork should not be underestimated. Hand-cut artwork can usually be made slightly more accurate than machine versions and is easier to modify for small changes. In either case the artwork should be made as large as possible, because the larger the artwork the greater the accuracy. Furthermore, larger artwork is easier to peel and check.

When peeling opaque "Mylar" or "Rubylith" material for the gate and/or contact layer, it's best to avoid positive-form artwork where the gates and contacts appear as small red spots on a clear background. When artwork in this form is rolled up for transport to the first reduction camera, it's very easy for one of these spots to fall off without being noticed. The resulting circuit, which almost works, causes frustration, lost time and added development budget expense. To preclude this sort of difficulty, it's best to use negative-form artwork where the gates and contacts appear as clear spaces on a dark background.

Once the artwork is cut to the required dimensional tolerances, there's no guarantee that these tolerances will be maintained unless certain precautions are taken. From the time the artwork is on the cutting table until the time it is photographed, it should always be stored flat and never subjected to violent changes in humidity. Finally, using high-intensity reproductions nets greater tolerance in light levels during mask reproduction—which also helps to hold dimensional tolerances.

Conversion of Artwork To Production Masks

The following are some common errors encountered regularly in masks being used and delivered today:

–Magnification error: Die image is not the same from one mask to another. This can be avoided if the mask maker carefully checks dimensions at each reduction stage.

–Rotation error: Die image is rotated with respect to the X and Y axes of the mask.

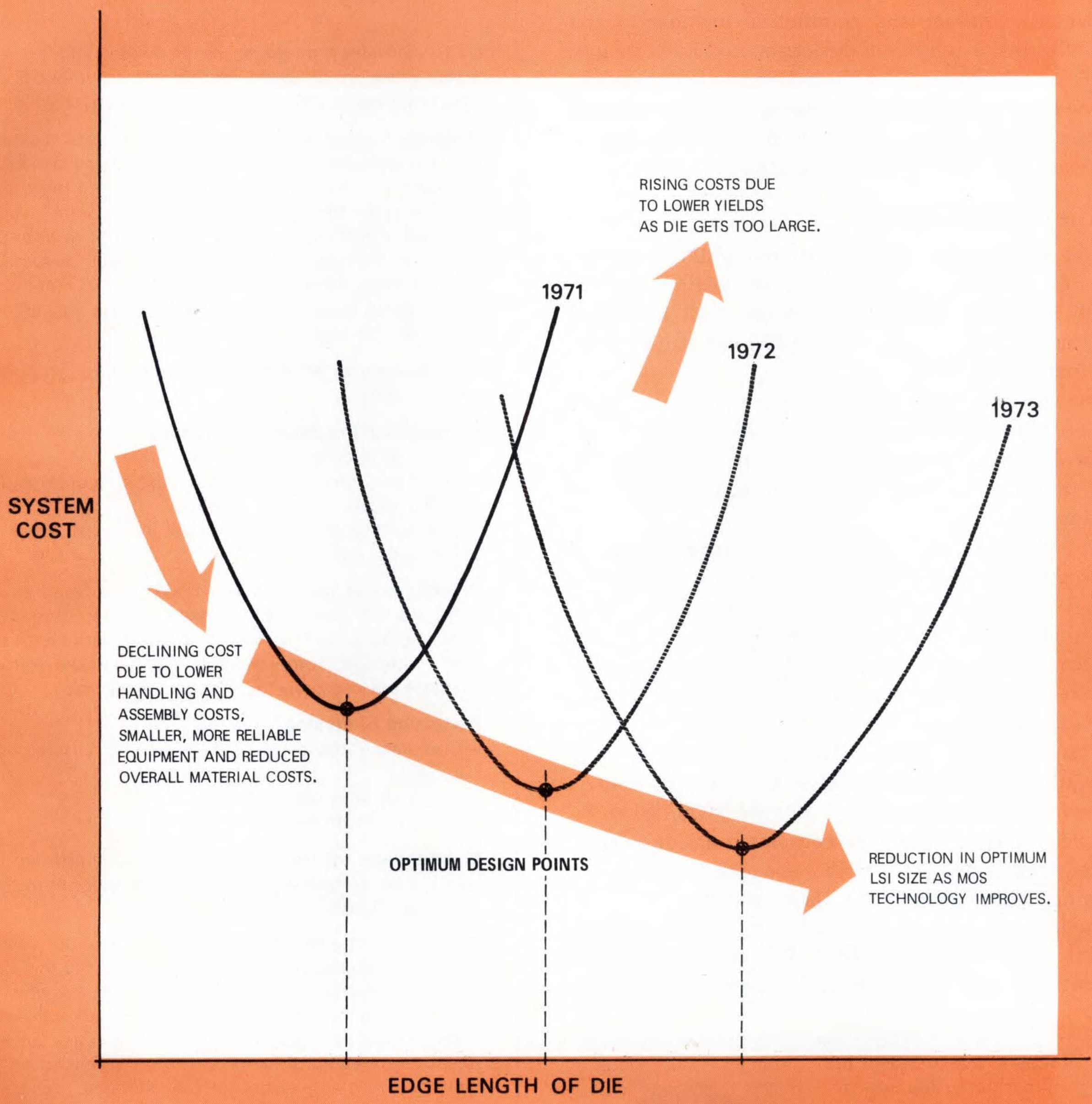


Fig. 3—**Optimum chip size** depends on cost per function. Cost per function depends not only on yield, but also on the handling and assembly costs of the good chips. Increasing the chip size can decrease the handling and assembly costs, but at the same time it can raise costs because of yield losses. The optimum chip size, therefore, is one that minimizes the sum of these two cost factors.

(Continued)

—Stepping error: Distance between rows or columns of devices differs from desired spacing. Best equipment for avoiding this is a fully-automated stepping machine.
—Runout: Gradual and cumulative increase in the size of a row or column of devices occurs. Even though mask alignment can be achieved over existing devices at the center of the wafer, increasing misalignment can be seen as the microscope is moved toward the edge of the wafer (for the same mask position).

In the Homestretch

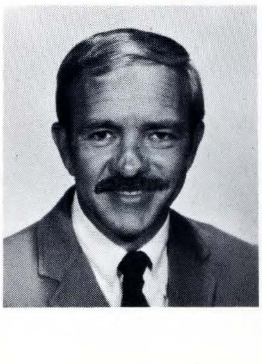
You might think once your brainchild has gone through the wafer processing and testing—and is nicely ensconced in its final package—that your yield worries are over. Not true! Yield loss can still occur in the final testing stage.

For example, packages with open pins can cause device failure. Of course, such bad packages can quickly be detected by a pin-check test, in much the same way that a probe-check test is performed during wafer testing.

One of the easiest ways to lose devices during final testing is by bending their leads while inserting them into a test socket. Bent leads can cause open pins and may damage the package. Though package carriers can reduce the occurrence of bent leads, it's more important to establish a correct operating procedure and provide regular supervision.

Unquestionably, MOS/LSI is the only way to go if an equipment designer wishes to maximize his contribution to his product design. But for MOS/LSI to be simple and economical, the equipment designer must understand as much as possible about the economics of making semiconductors. In short, the designer must always, from initial concept through final testing, "think yields." Today's $10 to $15 custom MOS/LSI circuit that can replace several PC boards full of circuits is well worth the effort. ▭

Mel Phelps is vice president in charge of marketing and sales at Nortec Electronics Corp., Santa Clara, Calif. He came to Nortec after 1-1/2 years as Vice President of Marketing with Fabri-Tek Corp. and 7 years with Fairchild Semiconductor, including 3 years as Product Marketing Manager for Fairchild ICs. Phelps is a graduate of Case Institute with a B.S.E.E.



Yields...
at the Wafer Level

MOS/LSI wafer processing can be divided into four broad areas: masking, diffusion, testing and assembly. Each of these processes is discussed below in terms of yield.

Masking. In most well-established processes, masking is the principal factor controlling yield. Furthermore, the incidence of mask defects determines to a large extent the size of die that can be used. A process that averages one defect every 150 mil^2 will generally have poor yield. However, that same process could, with reduction in mask defects, produce 75% yields on a 750 mil^2 chip. To obtain good yield, one should strive for the following mask-making goals:

Maintenance of all mask dimensions through photoresist and etching.

Perfection of the photoresist process. This includes:
—Good edge definition
—Freedom from pinholes, particles, scratches and distorted patterns
—Complete and adequate resist coverage (over high oxide steps, etc.)

Cleanliness of masks. Clean masks in a clean environment can still pick up photoresist particles from contact with slightly sticky wafers, and these particles are not easily removed from emulsion masks. Masks with hard surfaces are less likely to pick up such particles.

Perfection of etching. This includes:
—Complete removal of oxide without excessive undercutting
—Freedom from bubble effects
—Freedom from lifting

Maintenance of registration patterns between mask levels. Registration imperfections include both misalignment by operator and wafer warpage.

Diffusion. Diffusion failures lead to threshold voltages, breakdown voltage and p+ sheet resistances that do not meet specifications. Unlike masking defects which are localized, a diffusion failure usually ruins an entire wafer. Though diffusion failures occasionally cause an entire run to be rejected, they have less of an impact on yield loss than masking errors. In the diffusion process, dielectric deposition and metallization are the major factors that affect yields; these are discussed below:

Dielectric deposition. In dielectric deposition processes, non-uniform deposition and particle formation can be significant yield loss factors and can make masking steps more difficult.

Metallization. There are several factors in metal evaporation (the metal is generally aluminum) that influence yield.

—Probably the most important metal problem is inadequate coverage of oxide steps. In MOS processing, the relatively high oxide steps give rise to shadowing effects which can cause metal discontinuities. To minimize failure over these steps, one can use elaborate evaporation systems, substrate heating (which increases the surface mobility of the aluminum atoms) and oxide step tailoring.

—Metal masking problems related to the evaporated aluminum include: difficulty of defining patterns in the thick aluminum that is used to assist step coverage, variation in etching characteristics, missing spots and lumps. Of all the masking steps, the metal masking step probably has the most influence on final yield. Thus careful attention to the perfection of the aluminum layer is well worth the effort.

Testing. Significant yield loss is still possible during the testing phase. Some of the ways to minimize it at this stage are discussed below:

—Use a tester that performs both parametric and functional testing. By eliminating the need for double testing (i.e., testing once for function and once for parameters), you can halve the amount of handling required and thus halve the possibility of probe damage or contamination.

—Make sure that only highly skilled and properly trained operators are employed. Employing incompetent personnel often results in trouble from misaligned probes, improper loading, probe bounce and similar causes of lowered yields.

—Probes must be properly aligned. A misaligned probe can produce open or short circuits and result in a low or even zero yield. Possible misalignments should be avoided by including a probe test at the beginning of the electrical test sequence. Such a test checks for open and shorted pins, and alerts the operator when an excessive number of opens or shorts is encountered.

—Probe pressure should be properly adjusted. If the pressure is too light, the probe will be unable to do the job for which it was designed; if the pressure is too heavy, the probe can gouge the aluminum pad or even break the die.

—During wafer testing, chips are electrically sorted, and the rejects are "inked-out" so that at a later step they can be visually identified and removed. It is important at this stage to avoid ink splatter, because the operator charged with removing "inked-out" chips may remove good chips that have been accidentally splattered.

—The wrong program in the tester or wrong loading of the device under test can lead to device failure at the wafer sort. It is necessary to check the program and loading at the start of each shift by testing a standard wafer (a wafer with a known number of chips on it). The number of indicated good chips on the standard wafer should be the same as when previously tested. If it is different, the tester should be examined for defects.

—Keep the tester accurately calibrated. A calibration error can result in failure owing to small parasitic currents. This is especially true when measuring low currents (such as leakage currents on the order of 10 nA).

—Unwanted transient voltages and rough waveforms can cause good units to fail. The driver pin output should be periodically checked with an oscilloscope to see if such transients or waveforms are present. If they are, they can be eliminated by terminating the affected lines at the probe head.

—Keep the test area clean. Wafer contamination can reduce both yield and reliability. Always use tweezers—never touch a wafer with your hands. Wafers not being tested should be stored in closed boxes.

Assembly. There are many wafer assembly techniques, such as flip-chip, beam lead, chip and wire, etc. Each technique requires unique assembly equipment—hence each technique has unique yield problems. For discussion purposes, we will focus on the most popular assembly method: preformed die attach followed by wire bonding. Causes of yield loss during this type of assembly are discussed below:

—**Wafer Scribing.** If the tool gets dull or out of alignment, chipping or scratching of the die may occur. Losses of up to 10% from scribing errors are common for LSI chips. To prevent such losses, only properly trained operators should be used and tools should be inspected regularly.

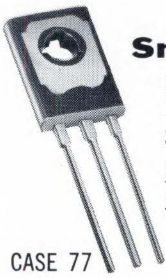
—**Die Attach.** If the machine is not correctly adjusted, there may be extra preform flaking, stressing and die damage or even no die attach at all. Therefore special attention must be given to the setting up and checking of the machine. Once set up, the machine should be checked at least once a day. Operators must be monitored constantly to make sure that they are not scratching the die, that they are "scrubbing" the die into place in the correct manner and that they are, in general, putting out quality work. Visual inspection of the finished work should be made once a day on a random basis. If good visual aids and well-written specs are not provided, or if the operators are incompetent, many good units may be discarded by mistake.

—**Lead-Bond.** If the machine is improperly adjusted, there may be loss of bond strength. An inspection should be made immediately following the start of each shift. Five to ten wires per device should be checked for bond strength. If the quality level is not high enough, the machine should be shut down and repaired. Bonding diagrams are essential to insure good continuity from unit to unit. The bonding tool must touch the bonding pad accurately. If the operator is moving too quickly or is not watching, the bond may be smeared or deformed, causing lower yield. Daily checks should be made to insure that the operator is building to the correct bonding diagram and that bond placements are correct.

—**Inspection Criteria.** Visual inspection tends to be subjective. Thus there should be photographs and drawings that depict various types of failure. Otherwise, an inspector might throw away good units in the belief that they were faulty. Even for a well-controlled process, a yield loss of 5 to 10% is common at this step.

—**Final Seal.** To insure a proper seal, sample units should be pulled off the sealer during the initial setup of the machine. Continuity of the weld or glass-ceramic seal should be inspected, and the entire unit should be tested to determine whether or not the hermetic seal is adequate.

Will The Designer Who Ordered Plastic Silicon Power In More Than One Package Size, Power Rating and Lead Form,

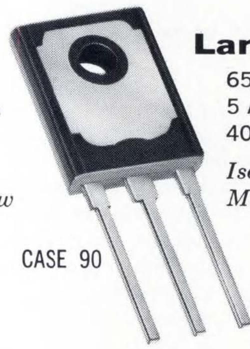


Small
10 to 40 W
100 mA to 5 A
30 to 350 V
Isolated Mounting Screw

CASE 77

Medium
30 to 90 W
100 mA to 10 A
30 to 350 V
Non-Isolated Mounting Screw

CASE 199



Large
65 to 100 W
5 A to 15 A
40 to 80 V
Isolated Mounting Screw

CASE 90

Please Drop It Right Into

It's Ready!
Thermopad* plastic power — now available in just about any size, power rating and lead configuration you require . . . for immediate drop-in into any metal-device socket you might have: TO-66, TO-5 or PCB, for flat or flag-mounting, with or without heat sinks . . . in high voltage, complementary EpiBase* and Darlington technology!

And you've got over 120 types to do it with: 33 registered and 90 house-numbered units that ensure your getting exactly what you need . . . eliminating over or under-design . . . without costing more than you want to pay!

You have your choice of 40 "small" case 77 types offering the most compact design possibilities . . . available in either E-C-B or B-C-E pin styles . . . readily replacing TO-66 units and furnished in 10 different lead forms.

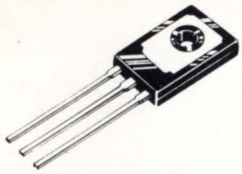
Use the newest, "medium-sized," case 199 to directly replace TO-66s and other plastic types with unformed leads where direct, metal-to-metal mounting screw attachment is desired. Like the case 77 and case 90, the 199 provides the most intimate heatsink-to-header contact seal in the industry and offers superior hermetic case integrity in high humidity environments. Power dissipation is also greater because of its 60% bigger heatsink area.

"Large" in every way, the case 90's minimum, .032″ thermal path length provides essentially the same θ_{JC} as a copper TO-3 in spite of the fact it has only one-fourth the heatsink surface area! You also get Darlington / complementary capability and up-to-100 W performance!

Get the whole story on Motorola plastic silicon power — write Box 20912, Phoenix, AZ 85036 and receive data sheets plus a copy of the new LEADFORMS brochure . . . it details dimensions, styles and applications of Motorola's unique capability to fit plastic power devices to any of your sockets. It's right now!

*TRADEMARK MOTOROLA INC.

CASE 77



Standard Straight Pin
E-C-B Pin Style

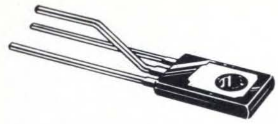
CASE 77

Standard Straight Pin
B-C-E Pin Style

CASE 77

TO-5 PCB Pin Circles
(Heatsink Optional)
Collector Bent
Away From Heatsink Surface

CASE 77

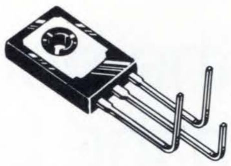


TO-5 PCB Pin Circles
(Heatsink Optional)
Collector Bent Toward
Heatsink Surface

CASE 77

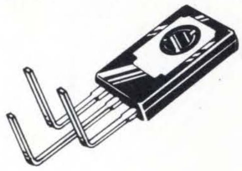
TO-66 Sockets
Standard Lead Length

CASE 77



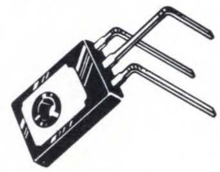
TO-66 Sockets
Long Lead Length

CASE 77



PCB Mounting
Trimmed Leads

CASE 77

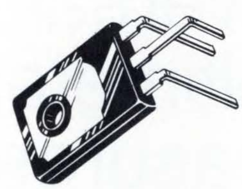


PCB Mounting
Heatsink Surface Down

CASE 90

Standard Straight Pin
E-C-B Pin Style

CASE 90

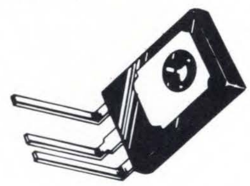


Flat Mounting On Heatsink

CASE 90

PCB Or Heatsink Mounting
Long Collector Lead

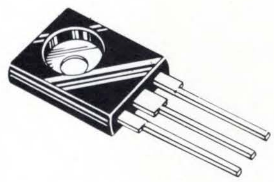
CASE 90



PCB Or Heatsink Mounting
Short Collector Lead

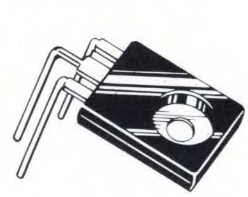
His Sockets.

CASE 199



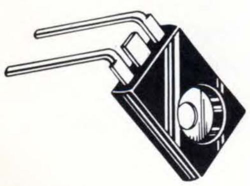
Standard Straight Pin
B-C-E Pin Style

CASE 199



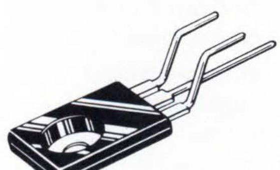
TO-66 Sockets
Electrically Integral Collector

CASE 199



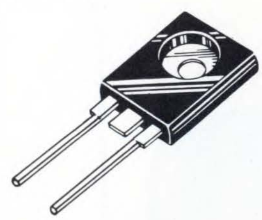
TO-66 Sockets
Trimmed Collector

CASE 199



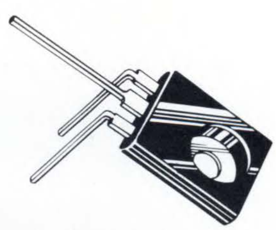
Popular Plastic
Flag Mounting

CASE 199



PCB Sockets
Flag-Mounting,
Trimmed Collector

CASE 199



TO-66 Sockets
Optional Center Lead Connection

CASE 199

PCB Sockets
Flat Mounting
Without Heatsink

3 Different Sizes,
19 Different Lead Forms To Choose From!

MOTOROLA POWER

In The First Place, It's Easy.

CIRCLE NO. 13

UNIVERSAL SPEED-POWER NOMOGRAPHS

To fully engineer modern digital systems, you should know the relationship between your logic circuits and the power they'll need.

CHESTER W. YOUNG

Here are three nomographs that will help designers balance their choice of logic type against the size and weight of the system power supply. As more and more variations of bipolar and MOS logic families are offered, it is easy to get bogged down by the tedious calculations needed to properly compare them. These charts reduce the effort required to relate a logic circuit's power dissipation to the circuit's parameters. Also, after a particular logic family has been selected, they can help determine what voltage level and clock frequency to use.

The first two nomographs are concerned with the basic components of dissipation, static and dynamic, and the third nomograph is helpful for determining power consumption in whole systems, such as LSI chips.

Total Gate Power

The total power dissipated by a gate operating at a given speed is the sum of its static and dynamic dissipation:

$$P_{tot} = P_s + P_d$$

where: P_s = the static dissipation that goes on whether the gate is handling a signal or not

P_d = the dynamic power dissipated in switching as the gate handles the signal

This and other equations that follow are from **Ref. 1**.

Static Power Nomograph

The static term, P_s, is a direct function of the power-supply voltage and an inverse function of the gate's supply-to-ground resistance:

$$P_s = \frac{(V_{pow})^2}{R}$$

where: P_s = gate static power dissipation

V_{pow} = power-supply voltage

R = effective supply-to-ground resistance of the gate (which may be different for the ON and OFF states)

Nomograph 1 solves this equation. It is a three-scale alignment chart that has a very wide range of values on the R and P_s scales to encompass the complete range of both current and expected bipolar, MOS and CMOS logic families. The power supply voltage scale goes from 1 to 50V, which should cover both the new

(Continued)

EQUATION TERMS		UNITS	BIPOLAR					MOS			
			1 ECL	2a TTL	2b DTL	3 28V DTL	4 Low Level	5 P-Channel	6 Complementary		
P_s	V_{pow}	V	5	5	5	28	2.5	12	10		6
	$(V_{pow})^2$		25	25	25	784	6.25	144	100		36
	R	kΩ	0.36	1.25	2	7	1.25M	300	10^{10}Ω		10^{10}Ω
	$= (V_{pow})^2/R$	mW	70	20	12.5	112	5 µW	0.5	10 nW		3.6 nW
P_d	C_L	pF	5	15	10	10	5	0.2	50	10	2
	V_{sig}	V	0.7	2	3	27	0.3	12	10	10	6
	$(V_{sig})^2$		0.49	4	9	730	0.09	144	100	100	36
	f	MHz	100	50	10	0.01	0.3	1	1	0.001	100 Hz
	$= C_L(V_{sig})^2 f$	mW	0.245	3	0.9	73 µW	0.1 µW	0.03	5	1 µW	7 nW
$P_{tot} = P_s + P_d$		mW	70.25	23	13.4	185	5.1 µW	0.53	5	1 µW	11 nW
$1/f_c = RC_L$		nsec	1.5×10^{-9}	18.75	200	70	6.25×10^{-6}	60×10^{-9}	1	10^{-1}	0.02
$f_c = 1/RC_L$		MHz	670	53	5	14	0.16	16	1	10	50
$f_{cross} = (V_{pow}/V_{sig})^2 f_c$		MHz	3400	330	135	15	11	16	1 Hz	10 Hz	50 Hz

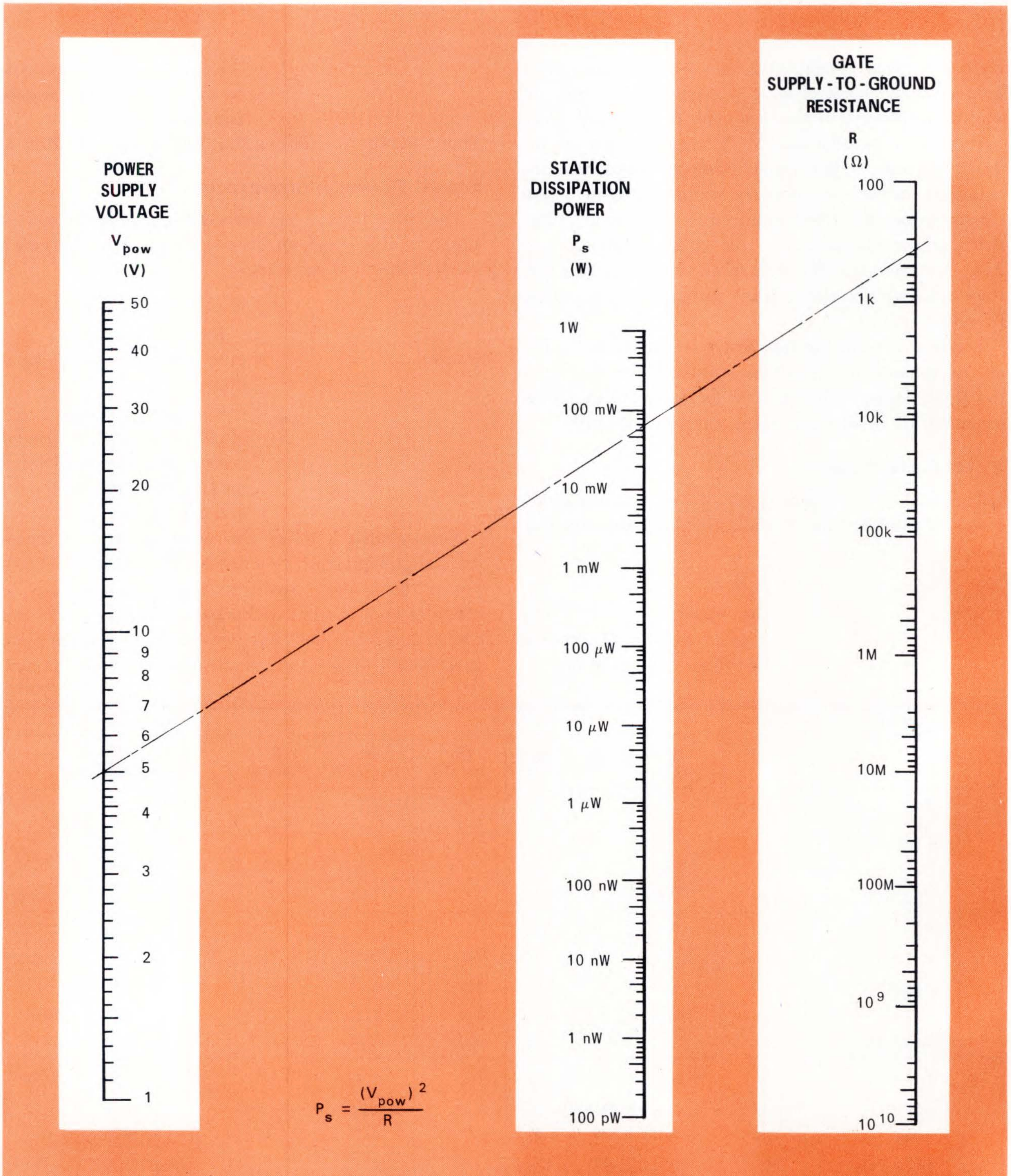
Table I—**Typical Gate Power Consumption** (from Ref. 1).

(Continued)

lower-voltage MOS wristwatch-type circuits and the higher-voltage industrial logic.

Example: ECL bipolar would have the following values (taken from Type 1 in **Table I**):

$$V_{pow} = 5\text{V}$$
$$R = 360\Omega$$
$$P_s = 70 \text{ mW}$$



Nomograph No. 1 — **Static Gate Dissipation**

A straight line drawn between the first two values (on the outside scales) intersects the center power scale at 70 mW, which agrees with the value shown in the table.

Many of the newer bipolar and MOS families have reduced static dissipation. Using this nomograph, it is easy to check the improvement in dissipation and to make comparisons between various brands. It is also a simple matter to see what benefit comes from operating a given logic at some other supply voltage. For example, in MOS memories the voltages are often reduced during standby to save power.

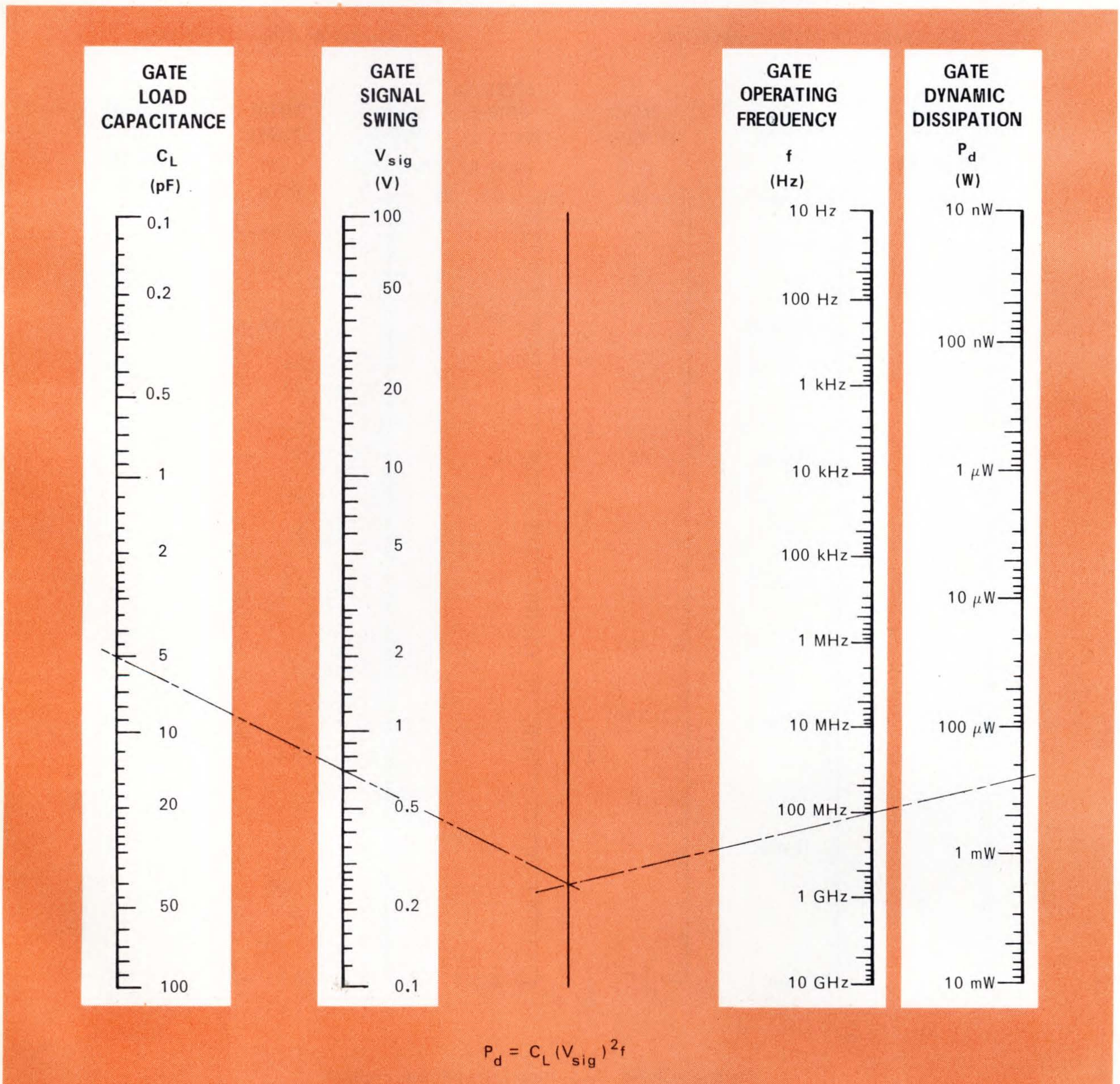
Dynamic Power Nomograph

The dynamic term, P_d, is a function of the capacitive loading at the gate's output, the voltage swing of the signal at the output and the switching frequency:

$$P_d = C_L(V_{sig})^2 f$$

where: P_d = gate dynamic power dissipation
C_L = load capacitance at the gate output
V_{sig} = signal swing
f = operating frequency

Nomograph 2, which solves this equation, is a five-



Nomograph No. 2—**Dynamic Gate Dissipation.**

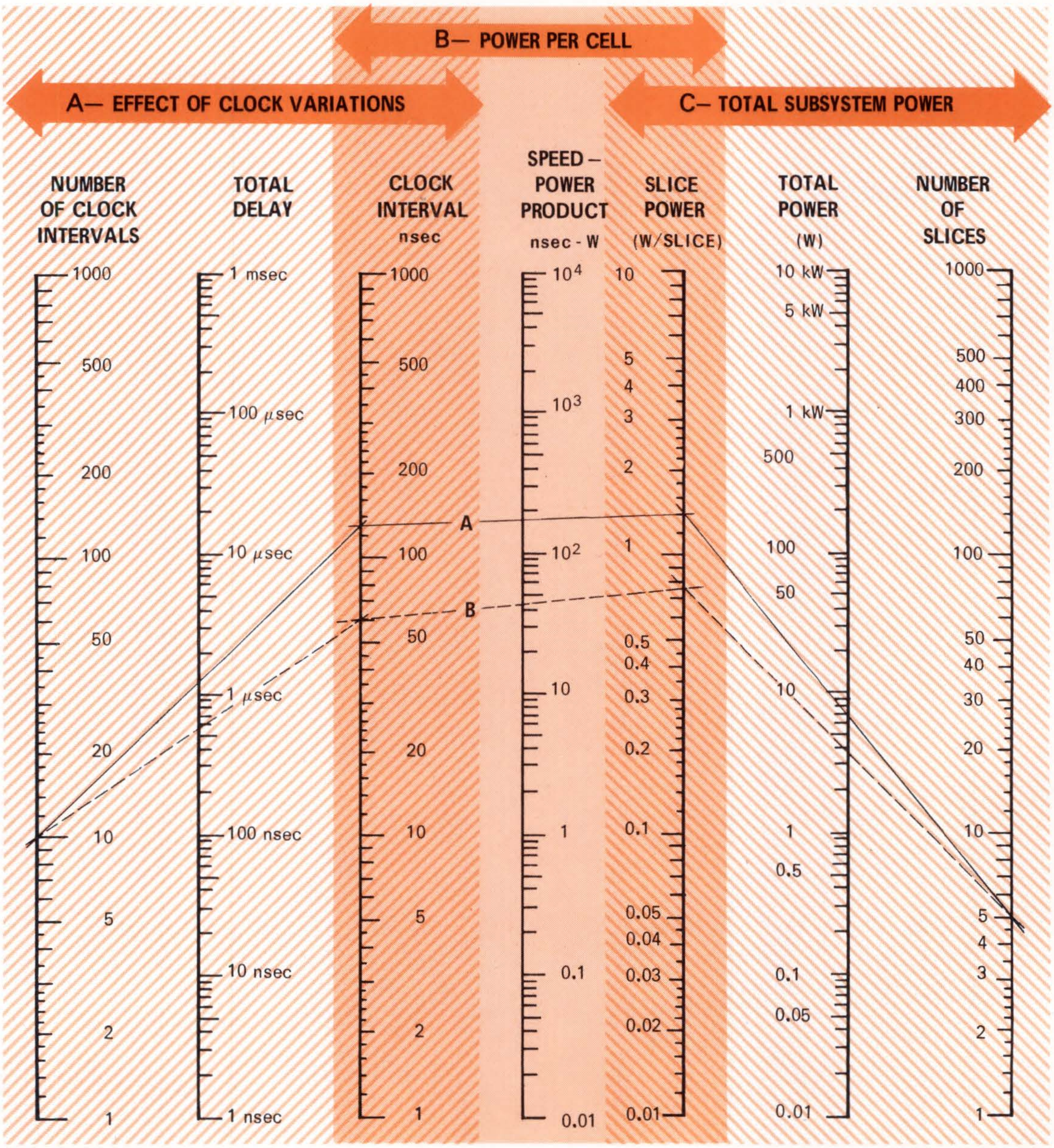
(Continued)

line alignment chart with four calibrated scales. It has one scale for each of the four terms in the equation, and a turning line in the center. A solution is generated by drawing a straight line through the values of the two parameters on the left-hand scales and extending it to the center line. From this intersection with the center line, a new line is drawn through the operating frequency and extended until it intersects the gate dynamic dissipation value on the far right-hand scale.

Example: For a typical ECL gate (Logic Type 1 in **Table I**), the pertinent value would be:

$$C_L = 5 \text{ pF}$$
$$V_{sig} = 0.7\text{V}$$
$$f = 100 \text{ MHz}$$

Drawing the lines (labeled 1) through these values gives a P_d of 245 μW.



Nomograph No. 3—**System Speed-Power Product.**

As can be seen from this nomograph, it really pays to keep the signal swing down if you want speed without using inordinate amounts of power.

Speed-Power Product for Systems

The third nomograph is for assessing the speed-power relationships in complete systems or subsystems. It helps you determine how close your system performance comes to the state-of-the-art. For example, it will help you compare a discrete IC implementation with a LSI version of the same system.

It assumes that you can break the system down into identical cells and that you know the power dissipation of each. It also assumes that you know the number of clock intervals to carry a signal through the cell and the time duration of each interval.

This nomograph is really three overlapping nomographs (A, B and C) side by side. Separate calculations can be made on either section and then extended, if desired, to the others.

On the left side (section A), the total delay is determined by multiplying the time of one clock interval by the number of clock intervals. On the right (section C), the total power is determined by multiplying the power-per-slide by the number of slices. This assumes that slice power is identical, or at least similar, from slice to slice. The examples are drawn from **Ref. 2**, which discussed a computer developed from general-purpose LSI arrays that had the uniformity implied by this nomograph.

Example: Here we compare a discrete IC implementation with a cellular LSI design. The discrete IC system has performance values of:

Clock Interval = 125 nsec
Slice Power = 1.4W

The speed-power product is determined from group B (middle). These values are located, plot A, on the third and fifth scales, and the line between them locates the speed-power product of 175 nsec-W on the center scale.

The total delay is determined from group A (left). If 10 clock intervals are assumed for this system, a line from 10 on the leftmost scale of A to the point on the clock-interval scale intersected by the previously-drawn line crosses the total delay scale at 1.25 μsec.

The total power is determined from group C (right). If the number of slices or cells (right-hand scale) is assumed to be five, then the total power scale is intersected at 7W.

Now you want to find out if you would benefit from going to some LSI scheme such as the "Uni-Cell" configuration discussed in **Ref. 2**, where all the silicon wafers are made up of repeating general-purpose cells. Because all circuitry is now compactly located on the same wafer, the clock interval or delay is reduced. At the same time, cell power is reduced because of the possibility of operating at lower voltages on chip and the decreased capacitive loading. The values for the LSI circuit are:

Clock Interval = 60 nsec
Slice Power = 0.75W

These LSI parameters reduce the speed-power product to 45 nsec-W (plot B), which is an appreciable improvement over the 175 nsec-W of the original discrete IC implementation.

Obviously, many questions must be answered about particular discrete and LSI circuits before you can come up with the values to plug into this nomograph, but the nomograph helps you get started by making clear which information you need.

Summary

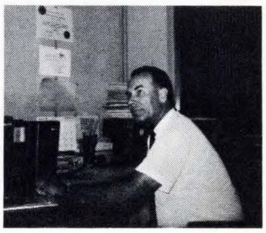
With these nomographs it is easy to compare the different device families. Such nomographs are especially valuable for comparison of new, improved, logic families as they are introduced. The new low-power TTL, the Schottky-clamped super-speed TTL, the ultraspeed ECL and the many new variations of MOS can all readily be compared for power dissipation by using these first two nomographs.

It is also possible to obtain some idea of how a given logic type will change with changing operating conditions. For instance, if you want to compare a number of alternative implementations of a logic equation with respect to power dissipation, you can draw the line for each variation on the chart and visualize the pros and cons. In this case, one of the principal variations will be the change of output capacitance with changing fanout. ▭

Databank

1. "Micropower: An Answer to the Power-Speed Trade-Off in Digital Systems," *EDN*, Aug. 1, 1969, p. 51. (Corrected version can be had as reprint L62 for that issue.)
2. "Fourth Generation Here Now," *EDN*, Nov. 1, 1969, p. 20. News story about a 4-bit computer register Raytheon built using Sylvania LSI "Uni-Cells."

Chester Young has worked for General Dynamics, Submarine Signal Co. and most recently, Walter V. Sterling, Inc. He says he has none of the usual hobbies like skiing or stamp collecting, but tends to spend a lot of his own time "exploring and reading about management techniques."



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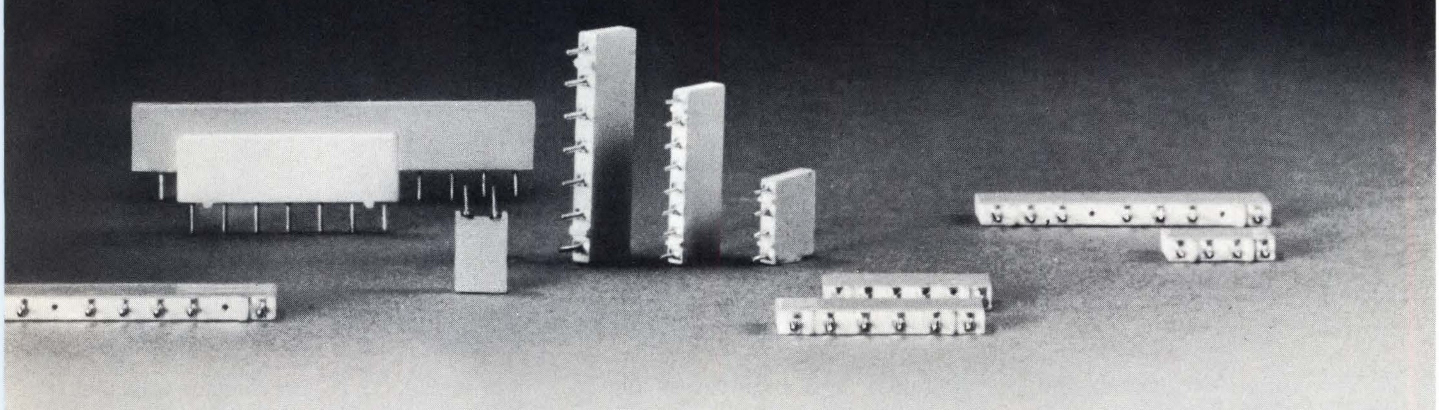

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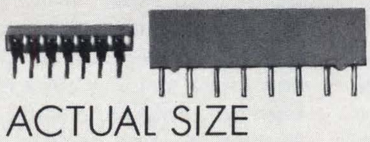


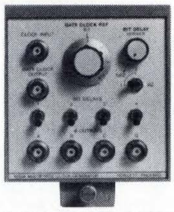
ACTUAL SIZE

CTS CORPORATION *Elkhart, Indiana*

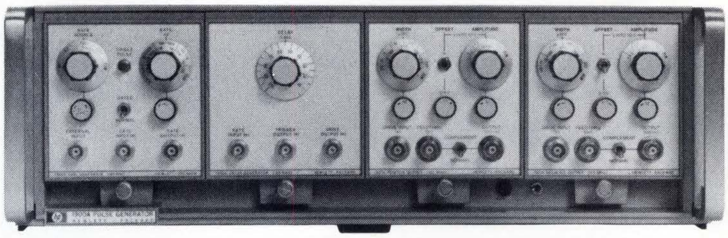
A world leader in cermet and variable resistor technology.

CIRCLE NO. 15

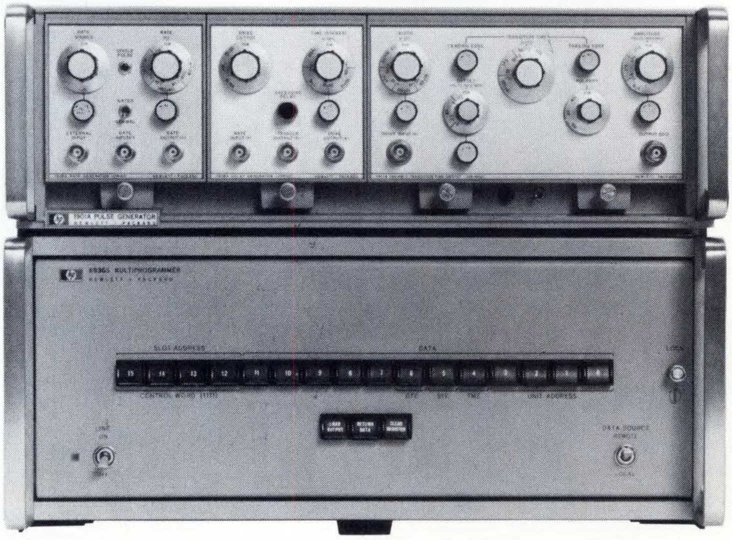
From HP—Three new dimensions in "pulser power"...



1. Multiphase MOS Testing



2. 125 MHz Capability



3. Digital Programmability

Hewlett-Packard's 1900 System, the pacesetter in pulse generation, now has three new capabilities that put it even farther ahead of all competitive pulsers.

1. Multiphase MOS Testing—The new 1934A Multiphase Clock plug-in lets you use the 1900 System to design and test MOS circuits with a minimum of effort. It gives you four-phase outputs to 12.5 MHz, or two-phase to 25 MHz...with variable phase pattern and variable phase overlap. The 1934A can be used with either high-threshold drivers (the 1915A) or low-threshold drivers (the 1917A); but the 1934A's price is strictly low-threshold...only $775.

CIRCLE NO. 24

2. 125 MHz Capability — Now, there are two 1900-System plug-ins that let you generate pulses at rep rates up to 125 MHz. The new 1921A (for positive pulses) and 1922A (negative pulses) are designed for testing fast T^2L and ECL logic—in computers and high-speed digital communications. Both have a fixed transition time of <2 ns, variable amplitude to 5 V, and variable ±5V offset. Both have switch-selectable complement capability, plus feed-through pulse-adding capabilities and pulse shaping capabilities. And both are compatible with other 1900-System plug-ins such as the 1930A PRBS generator. Yet you can get either the 1921A or the 1922A for only $950.

CIRCLE NO. 25

3. Digital Programmability — Now, your 1900 System can be computer-controlled, for high-speed automatic testing applications... thanks to HP's new 6936S Multiprogrammer. Its 16-line parallel input lets you interface your 1900 System to a computer quickly and easily, using only one I/O slot...and the result is a fully programmable pulser system suitable for almost any testing or control purpose.

To tie together your 1900 System and the 6936S, HP provides an interfacing package (Option 005), which includes cables, program cards and software. This lets you assemble the combination of capabilities best suited to your own particular needs. For example, you can get the 1900 with three popular plug-ins (1905A rate generator, 1908A delay generator, and 1917A variable-transition-time output) *plus* the 6936S Multiprogrammer and interfacing option 005, for $5950.

CIRCLE NO. 26

For further information on any aspect of the pace-setting 1900 System, contact your local HP field engineer. Or write Hewlett-Packard, Palo Alto, California 94304. In Europe: 1217 Meyrin-Geneva, Switzerland.

081/15

HEWLETT hp PACKARD

SIGNAL SOURCES

TESTING ANALOG MULTIPLIERS

Testing a multiplier is a difficult task because it is a nonlinear device. Here are some straightforward tests to determine just how close your multiplier comes to XY/10.

JIM H. PEPPER, Zeltex, Inc.

Analog multipliers have been essential to analog computers for years, but only recently have they gained popularity in the instrumentation and control field. The primary reason for the increase in usage has been the introduction of the low-cost small-package multiplier with reasonable accuracy.

Not only is specifying a multiplier difficult because it is a nonlinear device, but also industry-wide standards are lacking. This article points out the specifications that should be looked for and methods for testing such specifications.

BASIC SPECIFICATIONS

The most important specifications for a multiplier are:

1. Static or DC Accuracy
2. Dynamic Accuracy
3. Frequency Response
4. Step Response
5. Feedthrough Error
6. Input/Output Impedance
7. Tempco
8. Noise
9. Power Supply Voltage Coefficient
10. Differential Phase Shift

Additional specifications will be covered for the multiplier when it is used as a divider (or square root extractor).

Static Error

The analog multiplier should be a four-quadrant device that accepts time varying signals on inputs that have both positive and negative values with a maximum restricted to some reference voltage level. To specify the errors associated with all input values would be a difficult and costly procedure. In addition, temperature changes can modify the error pattern so that an entirely new set of information is required.

Static error can best be displayed on a 3-D plot of the error curve that can be represented on a 2-D plane. **Fig. 1a** shows such a plot. **Fig. 1b** shows the curve for an actual device. This display shows at a glance the effect of errors on static accuracy; it also allows extraction of linearity or other errors. If the error is displayed on such a plot, one can approximate the error at any input and also determine what quadrant or quadrants produce the smallest error.

Fig. 1b is an error plot for multipliers with smooth error curves, such as the pulse width/pulse height mul-

(Continued)

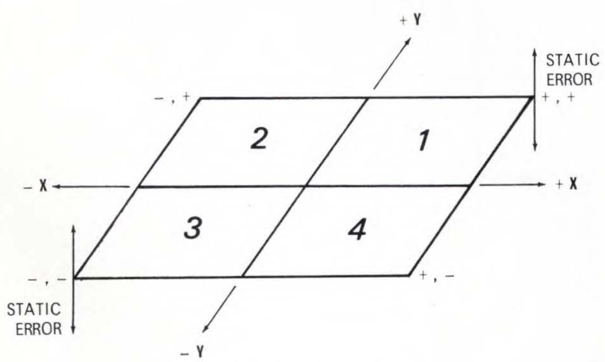


Fig. 1a—**Basic error plot.**

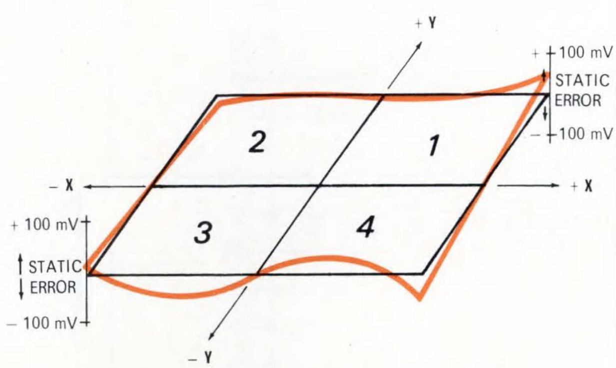


Fig. 1b—**Typical error pattern** for G_m multiplier.

(Continued)

tiplier or the variable transconductance type. The quarter-square multiplier that uses diodes and resistors to generate the square-law curve would have an error pattern of hills and valleys. The error of this type of multiplier may be as great when the inputs are close to zero as when the inputs are maximum values. The PW/PH and the Var G_m type have error patterns that become smaller as the input signals are reduced.

Note that the error for either input being zero and the other varied produces an error curve that reduces as the signal approaches zero.

Basic Test Setup

The circuit used to generate the 3-D plot is shown in **Fig. 2**. Although the above curve could be plotted by taking the errors at various points and plotting them, the use of the circuit in **Fig. 2** provides a better understanding of the 3-D plot.

Amplifier number 2 is needed when the output of the multiplier is negative because one input or the other is negative. All combinations of inputs should be tested at both zero and maximum values. The error curve can now be plotted, using this information, on the plot shown in **Fig. 1a**. By extrapolation, errors in regions other than maximum signal or zero can be approximated.

A check of the output error when both inputs are varying can be made, but the output must be compared to a device that is at least an order of magnitude more exact than the unit being tested. This test, known as the square-law test, is nonlinear.

With the information obtained from the above tests, the error in the divide mode can be approximated. The divide error is equal to the reference voltage divided by the Y signal level times the error of the multiplier at the point of operation (not the maximum multiplier error).

$$E_{Divide} = \frac{V_{Ref}}{Y} E_{Mult}$$

External Adjustments

In order to keep static error to a minimum, some manufacturers provide for external adjustments. It is very important that provisions be made for external adjustments if the multiplier is to be operated at any temperature other than that at which it was calibrated (usually 25°C). The Var G_m type multiplier typically has a spec of 3 to 5 mV/°C, and a 10°C variation could produce an additional error of 0.5%. An offset adjustment is of particular importance, since any error at zero times zero represents an infinite absolute error.

Adjustment capabilities for offset, X null, Y null and gain should be provided to take care of parameter variations in special situations, such as obtaining optimum results in divide, even though they may not be used

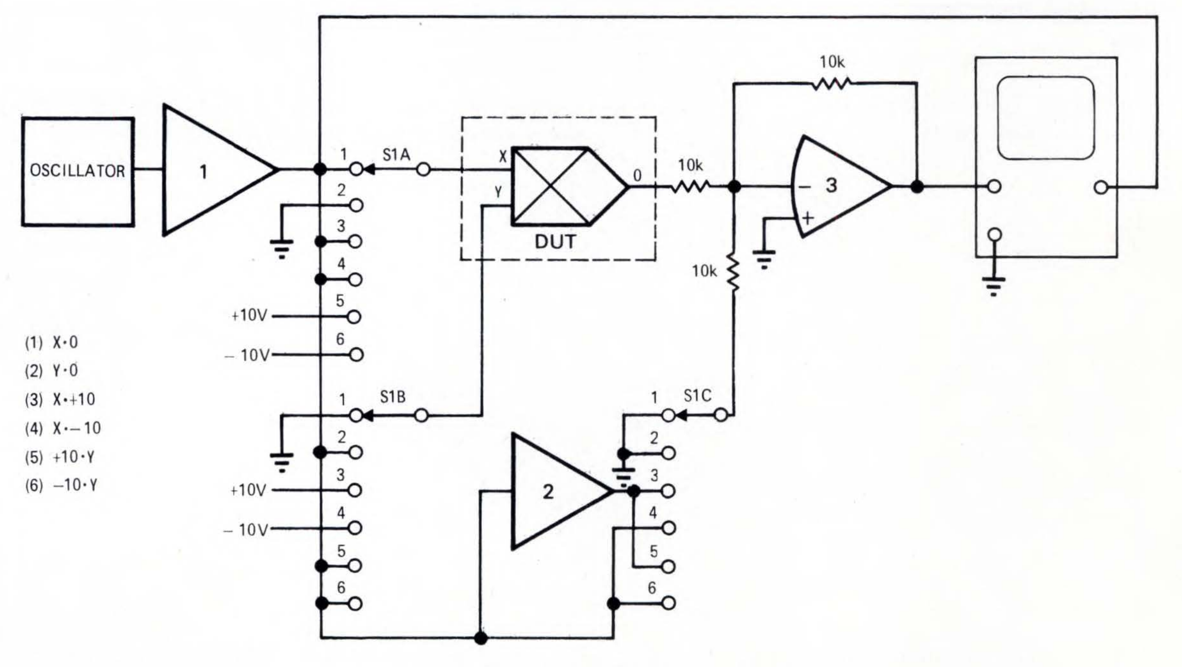


Fig. 2—**Circuit** for multiplier error plot.

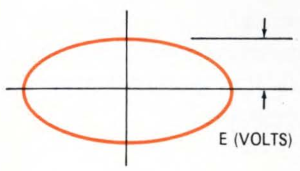


Fig. 3—**Phase measurement.**

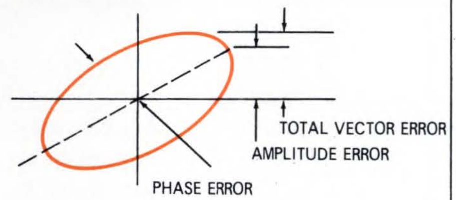


Fig. 5—**Amplitude-phase error.**

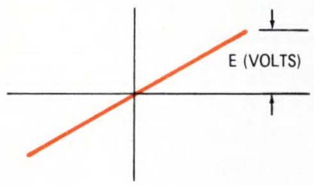


Fig. 4—**Amplitude error.**

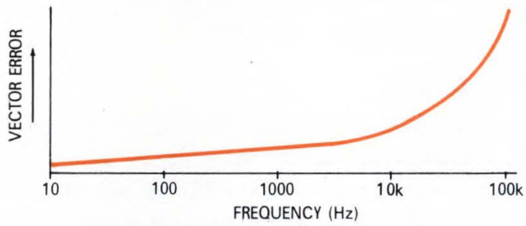


Fig. 6—**Error vs frequency.**

when multiplying.

Dynamic Error

The dynamic error includes both amplitude and phase error. In many applications, the static error is of secondary importance to errors at frequencies other than zero. Since the output of the multiplier is a product of two signals, to check its accuracy it is necessary to compare its output with a device that is at least one order of magnitude better than the device under test. The Var G_m type could be compared to a wideband high-accuracy, quarter-square multiplier up to about 5 kHz. Above this frequency it is difficult to determine the source of errors. A digital computer comparison falls apart at a much lower frequency. A 1-μsec propagation or calculation time is equivalent to a 1° phase shift at 5 kHz. An alternate to the above method is to convert the multiplier into a linear device by holding one of the inputs constant and varying the other.

Given $$E_0 = \frac{XY}{10}$$

let $$Y = 10$$

then $$E_0 = X$$

and the output can be compared directly with the input for all frequencies of operation.

The circuit used to determine the static error (**Fig. 2**) can also be used to generate dynamic statistics.

If the multiplier is operated at full amplitude on one input and the other input is held at plus or minus the reference voltage (generally 10V), the phase error can be measured in the following manner.

Phase Measurement

The phase angle (**Fig. 3**) can be obtained by

$$\phi = \frac{E\ 57}{V_{Ref}}$$

if E is in volts (good for phase angles less than 10°).

If the error pattern exhibits no phase shift but is tilted from the horizontal as shown in **Fig. 4**, the error is an amplitude error.

If the pattern exhibits both phase and amplitude error, the measurement should be made as in **Fig. 5**. The vector error can also be measured from this pattern.

These tests should be made for all combinations of inputs and should be plotted as shown in **Fig. 6**.

It will be noted in such tests that the predominant error at low frequencies is amplitude error with a typical crossover point about 10 kHz. This test should be made under no-load and full-load conditions.

The above technique can be used for amplifiers as well as multipliers since the multiplier is operating as a linear device.

Frequency Response

The frequency response of the full power output signal is of importance, because it indicates where the amplitude error starts to increase rapidly. To give the small signal −3 dB point is of little importance unless the total frequency response curve is given. It is quite possible to produce a wideband multiplier by including peaking in the response curve. The single specification

(Continued)

of the -3 dB point is then insufficient. Peaking in the response curve introduces instabilities if the multiplier is inside a feedback loop or is used as a divider.

Also, large overshoots caused by step function inputs will be produced. Peaking may also indicate poor capacitive load capability. Frequency response measurement can be made with the circuit shown in **Fig. 7**. Phase shift data taken previously can also be plotted on the same sheet.

The multiplier is a four-quadrant device and therefore should be evaluated for all combinations of inputs. When both inputs are being varied, the output is twice the input frequency plus a dc offset.

Step Response

Considerable information about frequency characteristics of a multiplier can be obtained by applying a square wave signal to the input. The response to the step function can give information on peaking as well as settling time. Here again, the various combinations of inputs should be evaluated. The circuit of **Fig. 7** can be used with a square wave signal substituted for the sine wave.

Various levels of square wave input signals should be supplied since excessive overshoot will probably occur only on small signal inputs.

At this time, the ability of the multiplier to drive a capacitive load can also be tested. A set of capacitors ranging from 100 to 1000 pF (a capacitor decade box is not always a good checking device because of inductance) can be applied to the output and the resultant square wave response noted. This test should also be made for various levels of input signals.

Feedthrough Error

Feedthrough error, sometimes called null error, determines the ability of the multiplier to reject a signal if the other input is held at zero as shown in **Fig. 8.** Ideally, the output should be zero when either one or both of the input signals are zero regardless of the frequency of the applied signal. Naturally if both signals are zero, frequency is of no concern. The typical Var G_m type multiplier varies from 50 to 100 mV peak error at 10 kHz when one of the inputs is maximum and the other is at zero.

Input/Output Impedances

This information is generally given but information about the driving impedances is usually lacking. It may not be simply a case of requiring a low driving impedance because of a low input impedance. A simple test is to ground both inputs and check the output voltage. Then open one input or the other and note any change in output. If large changes occur, the input must be driven from a low impedance source. For best results, it is considered good practice to drive the multipliers from outputs of amplifiers rather than through potentiometers or resistances.

Tempco

The Var G_m and pulse width/pulse height multipliers, being solid-state devices with some portions of the circuit operating open loop, depend upon tempco matching to reduce effects of temperature variations. Two specifications are generally given:

1) The zero times zero tempco in mV/°C
2) The gain tempco in %/°C

The latter is given as a percentage because the error of the multiplier is usually given in percent. To eliminate any possible misunderstanding, voltage should be given for this specification as well.

The measurement of the dc offset as a function of temperature simply requres an oven and a voltmeter. The inputs are tied to ground, and the change in output voltage as a function of temperature is measured.

The gain error (which includes offset error) should be measured at all input conditions and the offset error should then be removed. **Fig. 9** shows circuit configuration for TC measurement.

Noise

Noise is a random error that restricts the lower level of operation of the multiplier. This specification is generally given in rms volts. Again, noise should be measured with various inputs to obtain the maximum figure.

Power Supply Coefficient

The solid-state electronic multiplier may be very sensitive to voltage variations unless internal regulation is provided. This parameter variation should be performed with various inputs to X and Y to determine the exact sensitivities.

Differential Phase Shift

If the multiplier is to be used as a phase detector, the error introduced by the multiplier should be held to a minimum. The product of $X \sin \omega t$ and $Y (\sin \omega t + \theta)$ produces an output of $(XY/2)$ $[\cos \theta - \cos (2\ \omega t + \theta)]$. The first term is the useful or dc term. The second is twice the input frequency and can be easily filtered out.

Testing a multiplier for this specification for small angles is not easily accomplished. A differential voltmeter used as shown in **Fig. 10** should be adjusted to 5.000V for a signal input to the multiplier of 10V peak. ($E_o = (X^2/20) \cos \theta$ where Cos θ equals 1 for zero degrees

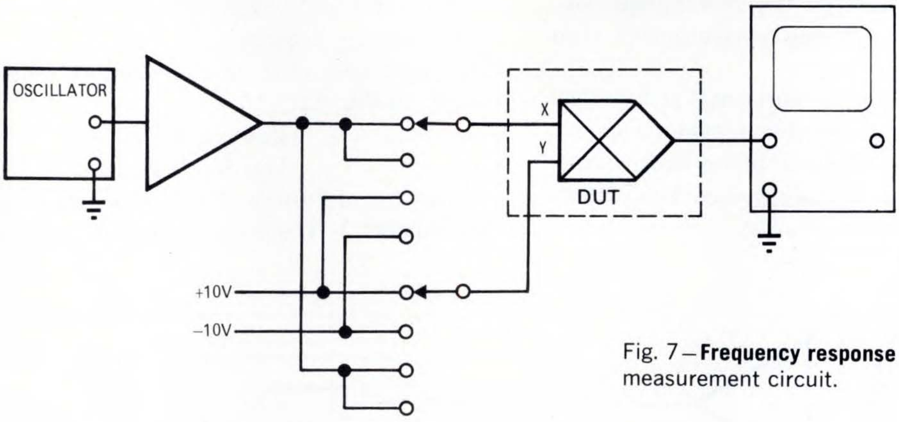


Fig. 7—**Frequency response** measurement circuit.

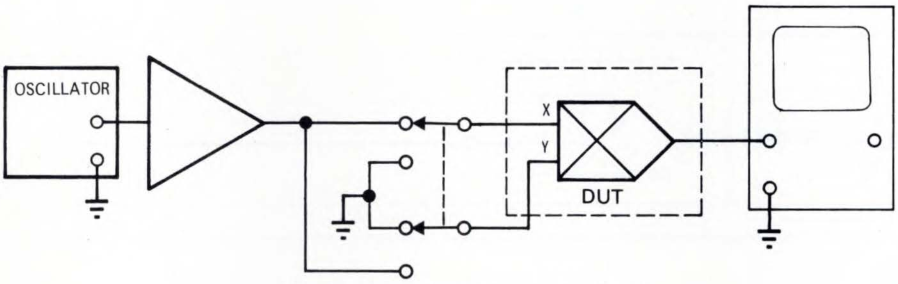


Fig. 8—**Feedthrough error** circuit.

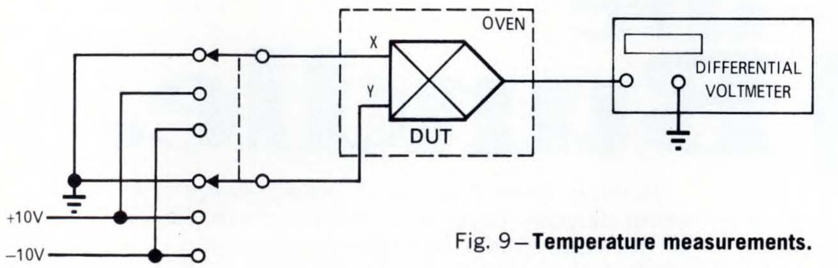


Fig. 9—**Temperature measurements.**

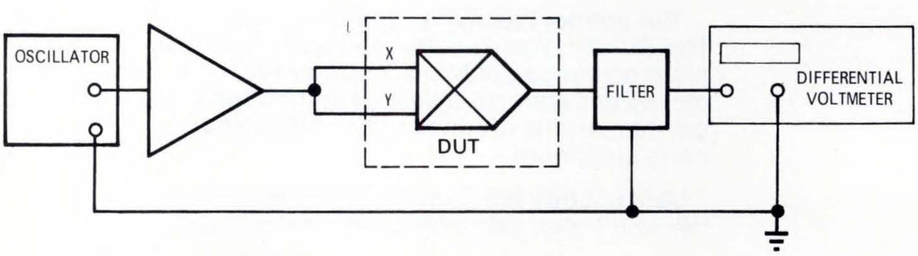


Fig. 10—**Differential phase shift measurement.**

(Continued)

giving a multiplier output of 5V.) Amplitude variations from the oscillator and from the multiplier restrict the method to a small range of frequencies. One degree of phase shift is equivalent to a 0.01% change in input amplitude, thereby making it difficult to resolve anything less than this. In addition, the cos θ changes very slowly in this region rendering measurement even more difficult.

Another method is to use the horizontal and vertical inputs of an oscilloscope. Care must be taken to assure that both channels have identical phase shift characteristics or this will lead to inaccuracies. The pattern generated will be a square-law curve.

Divider Operation

Tests that can be performed in the divide mode of operation are:

1) X divided by Y where Y = max and X is varied from plus to minus reference voltage
2) X divided by Y where $X = Y$
3) Frequency response

The static tests of (1) and (2) can be performed by the circuit in **Fig. 11**:

Position A Test 1
Position B Test 2

The error of Position A should be small regardless of the value of X. The error of Position B will increase as

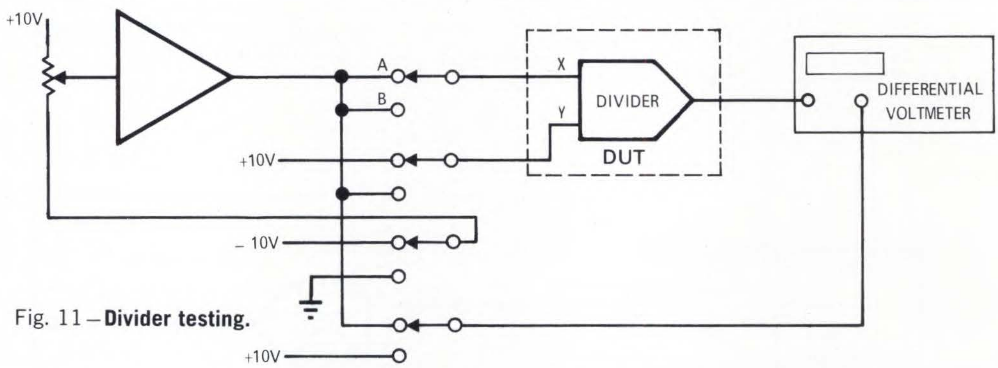


Fig. 11 – **Divider testing.**

the value of X and Y approaches zero and go to infinity (limited by saturation) when X and Y are zero. During this test a scope can be used to observe the noise level. A plot of this error might appear as shown in **Fig. 12.** The error follows the relationship $E_{divider} = V_{Ref}/Y\ E_{multiplier}$ as previously indicated.

Frequency Response in Divide

Because of the method used to obtain a divider configuration, the bandwidth reduces as the amplitude of the divisor reduces.[1] The method of testing BW is shown in **Fig. 13.** When Y is reduced, the multiplier acts like a feedback resistor that is increasing in value. The combination of internal C and the equivalent R of the multiplier thereby reduces the bandwidth. **Note:** The peak value of the X input must be held equal to or less than the value of Y. □

[1] *See Multiplier Applications Bulletin No. 1063B, Zeltex.*

Jim Pepper came to Zeltex, Inc., Concord, Calif., with over 14 years of experience with analog computers. He is currently an applications engineer. A graduate of the University of California, Berkeley, Pepper holds a B.S.E.E., has one patent to his credit and is a member of IEEE.

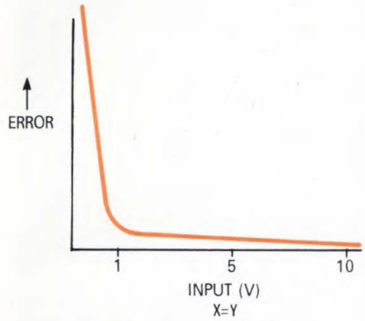


Fig. 12—**Divide error curve.**

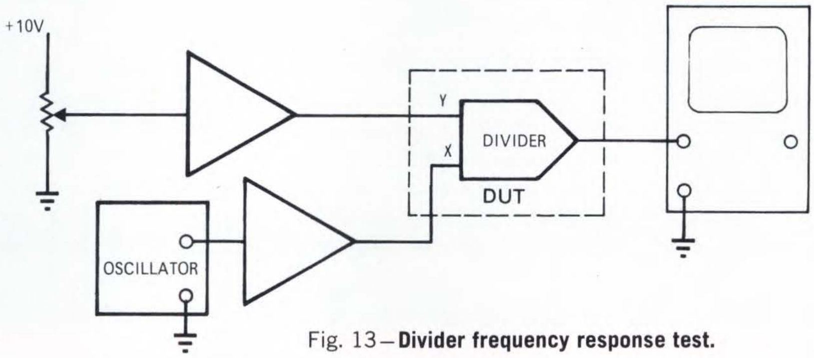


Fig. 13—**Divider frequency response test.**

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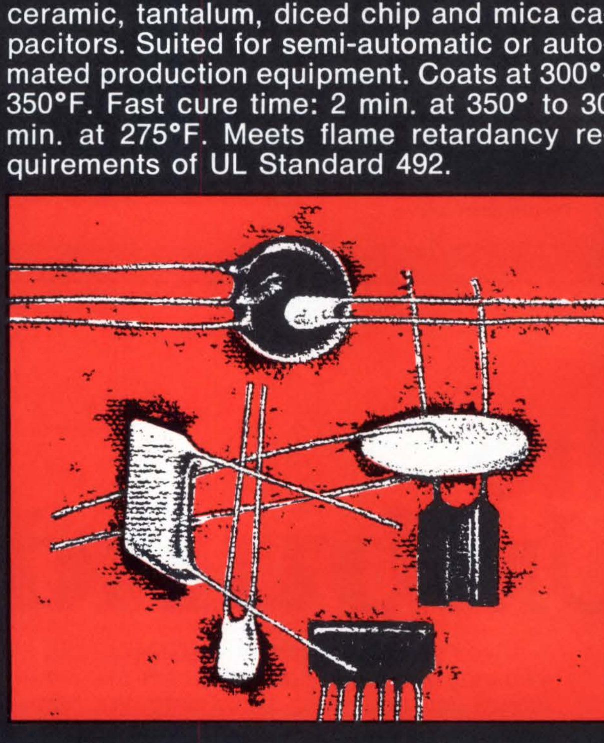

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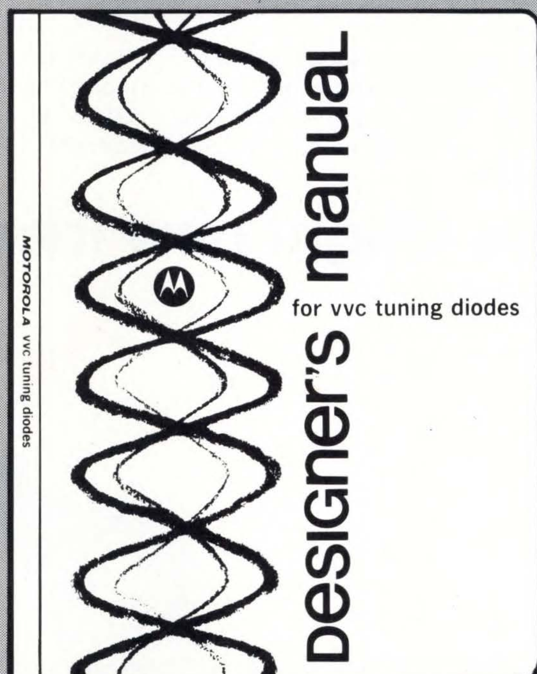

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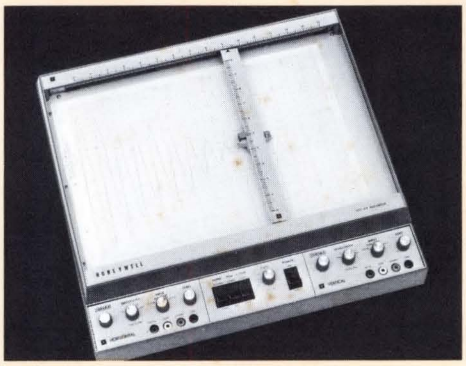

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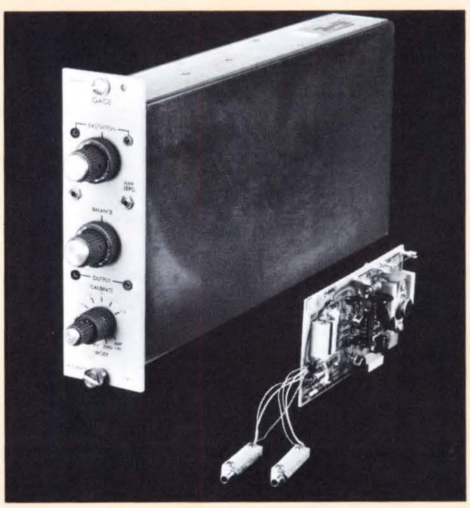

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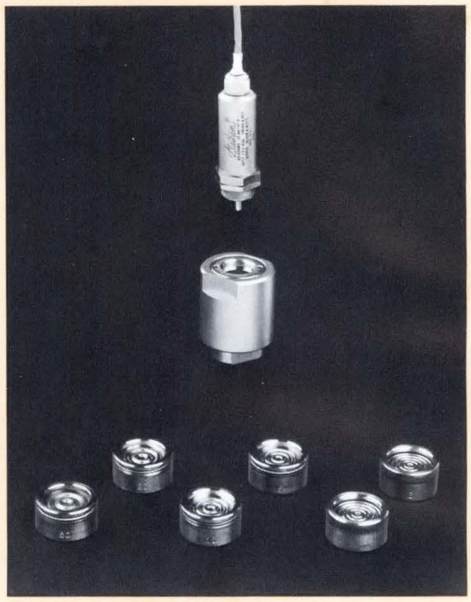

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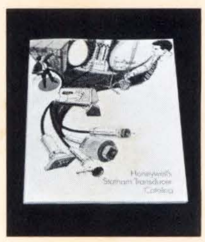

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Most electronic designers working with audio amplifier or general operational circuitry would like to have a phase meter covering the audio to 1 MHz range for making Bode plots, but the cost is usually prohibitive.

A general purpose meter is described here that has reasonable accuracy for most Bode plots and an IC cost of about $16.

Making Square Waves

Phase shift between two sine waves can be accurately determined if their zero crossing points can be found and compared on a time base. The equivalent of this is to square the waves, **Fig. 1**, and compare the amount of overlap T_2 to the total period T_1. This gives directly the amount of phase difference between the wave trains. In the limit $T_2 = \frac{T_1}{2}$ which yields the maximum phase difference of 180°.

Rather than measure periods, which can be tedious and time consuming, it is easier to integrate the period T_2 over the total period T_1. This gives an average of ON to OFF times, with suitable circuitry, which can be read on a voltmeter. A block diagram of the system used to accomplish this is shown in **Fig. 2**.

ICs Make It Work

Although the fundamental approach is simple, there are a number of difficulties in implementing the design. If the design goal includes detecting at levels as low as 1 mV rms, then present day comparators of the 710 variety exhibit too much offset and insufficient gain to function properly. Additional preamplification before the comparator solves the sensitivity problem and minimizes offset but introduces a whole new set of possible inaccuracies. These stem from the fact that as the amplifiers are driven into saturation, the duty cycle may vary considerably from the expected (and necessary) 50%. A good amplifier for the preamp and squaring functions is the Motorola MC1430G op amp because its speed and gain suit the application very well.

A second and equally important consideration when choosing the amplifier/squaring circuit is that no small-signal poles or zeros fall within the bandwidth of interest. These singularities cause phase shift at linear amplification levels, but may cause little or none at saturation levels. Even if the two channels are identically matched for small-signal phase shift, the overall error will increase greatly if one channel goes into saturation and the other does not.

The basic amplifier circuit used in the design of this meter is shown in **Fig. 3**. A Bode approximation for the linear response of this circuit (**Fig. 4**) shows that for frequencies above $\omega = A_{vol}/RC$, the gain is essentially the amplifier's uncompensated open loop gain. However, if we are to abide by the rule that no poles exist below 100 Hz (lowest design frequency) then the RC time constant needed would be:

$$\frac{A_{vol}}{RC} = 100\ (2\pi)$$

$$RC = \frac{A_{vol}}{100\ (2\pi)}$$

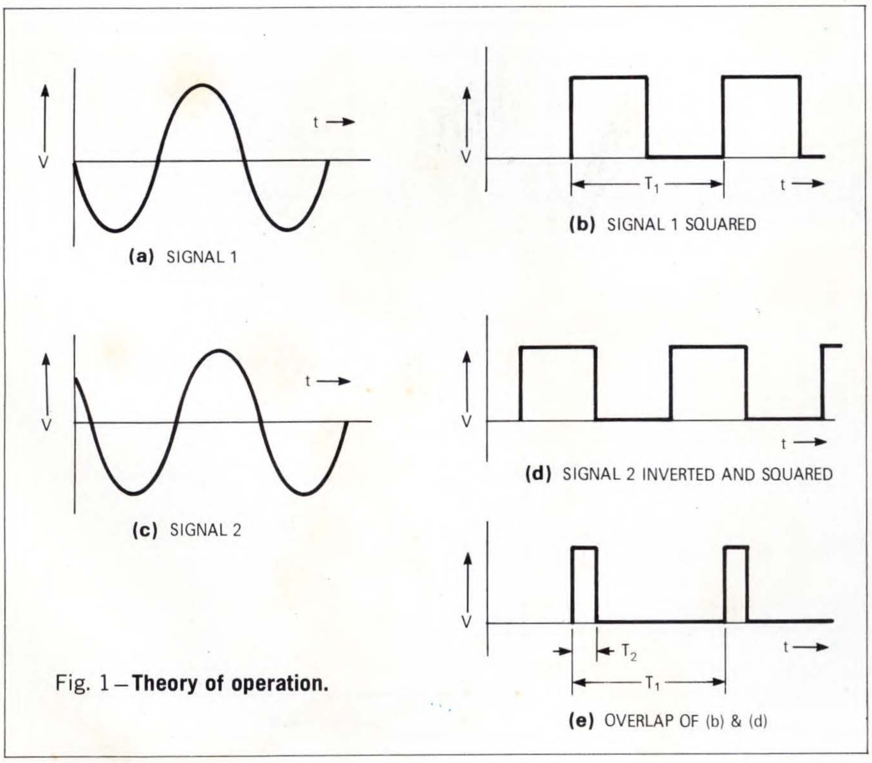


Fig. 1—**Theory of operation.**

(Continued)

Bias current considerations limit the value of R to about 100 kΩ. Open loop gain is about 5000. Using these values to calculate C:

$$C = \frac{A_{vol}}{100R\ (2\pi)}$$

$$C = 79.6\ \mu F$$

If C were chosen to be just this minimum value, phase shift at f = 100 Hz would be 45° (A_{vol} = 5000) and therefore the maximum possible error, assuming widely different levels, could be 45°. Input saturation level for the MC1430 at the supply voltage indicated is about 2 mV. Above this input level the phase shift should begin to disappear. To test this phase shift in the meter, a 100-μF capacitor was used as the feedback capacitor and a plot of error (degrees) vs frequency was taken for two input levels, 10 mV and 50 mV, with 20 dB attenuation between channels. At 10 mV one amplifier was in saturation and the other was not, and an error of 22° was realized at f = 100 Hz. When the input level was raised to 50 mV, however, both amplifiers produced close to zero phase shift and the error was only 6.3°. For low levels, it's clear that a relatively large valued, low voltage unit is needed for C.

The dual comparator used (to cut parts count) has adequate speed when overdriven as it is nearly all the time. Likewise the TTL AND gate performs the "overlap" function very well and leaves three unused gates for other purposes. Package count could have been reduced if the strobe capability of the MC1414 had been used, but it has the undesirable property of a small output level shift when being strobed OFF. This integrates into a small error angle. Output of the MC3001 is relatively undisturbed until both inputs are high.

An ordinary two-section RC filter is used as the integrator, **Fig. 5**, and is followed by a noninverting amplifier stage with a gain of about 3. All offset trimming, primarily necessary due to the MC3001 OFF state, is done at this amplifier. A variable resistor is the coupling element to the output buffer. The output may be measured either directly with a voltmeter or with a milliammeter connected through a resistor. In this mode the second amplifier is operated as a current buffer.

Setting It Up

Initial setup adjustments are necessary for offset trimming the MC1430s and the MC1414 to insure that high level zero crossings are the same as low level. Secondly, the TTL gate output is balanced to zero in the dc amplifier to represent zero degrees, and thirdly, the gain factor is set so that the output coincides with some conventional scale (for example, V_o = 1.8V for a phase shift of 180°). A step-by-step procedure is as follows:

1. Set an audio generator to 1 kHz, 2 mV rms and connect to the input of channel 1. Attach an oscilloscope to test point 1 and adjust R_1 until the duty cycle shows equal ON to OFF times.

2. Attach oscilloscope to test point 2, audio generator to input of channel 2 and vary R_2 until an approximate 50% duty cycle is obtained. (Note: It is advisable to connect the input of the unused channel to ground when

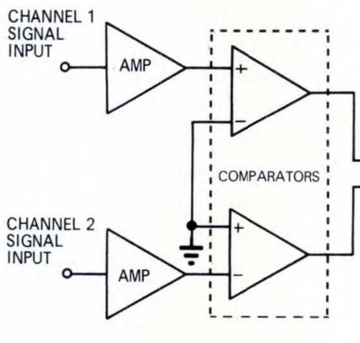


Fig. 2—**Block diagram.**

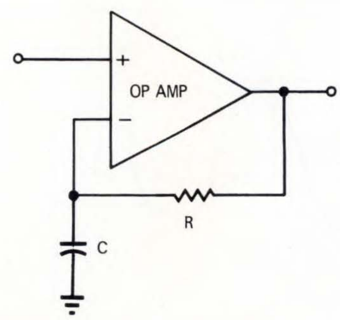


Fig. 3—**Basic preamplifier circuit.**

TABLE 1
SPECIFICATIONS

Effective Input Voltage Range:	2 mV to 1V rms
Power Supply Voltages Required:	±6V, ±10% +12V, ±10%
Phase Range:	±180°
Accuracy:	Error <3° (<2%) $V_1 + V_2$ = 5 mV Error <3° for V_1 = 20 mV V_2 = 2 mV 100 Hz to 100 kHz Error <10° (5%) for V_1 = 20 mV V_2 = 2 mV 100 Hz to 1 MHz

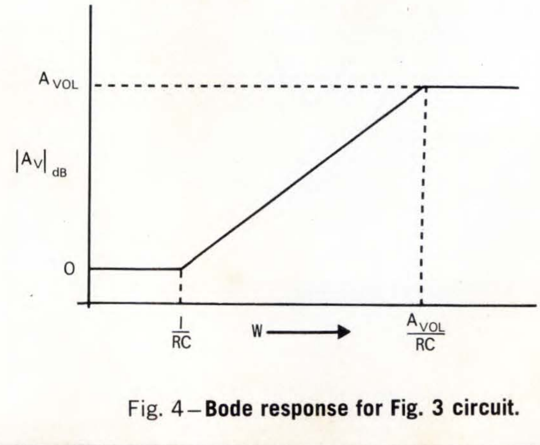


Fig. 4—**Bode response for Fig. 3 circuit.**

performing these adjustments.)

3. With the oscilloscope in the "add" function, connect scope probes to both test points and audio generator to both inputs. Minimize pulse width (overlap) by adjusting the offset in channel 2 (R_2) such that only slight spikes if any remain. See **Fig. 6.**

4. Adjust gain potentiometer (R_4) to maximum gain and set S_1 to position 1. Trim offset adjust (R_3) until output is zero. Turn S_1 to position 2 and adjust R_4 to read desired full scale at 180° of phase shift.

5. Repeat steps 3 and 4 while increasing the spike width until output is about 1% of full scale to insure that no "dead" zone exists.

Performance specifications are summarized in **Table I**. Channel matching for equal input levels is quite good owing primarily to the high gain which rapidly drives the devices into saturation.

Of equal importance is performance when input levels between channels are different. **Fig. 7** shows error for 20 dB attenuation between channels. Large shunt feedback capacitors (1000 μF) are used in the preamps to minimize error at low frequencies.

High frequency error (>100 kHz) is largely attributable to the differences in device switching speed vs voltage drive level. Even at several hundred kilohertz, however, error is still with-

(Continued)

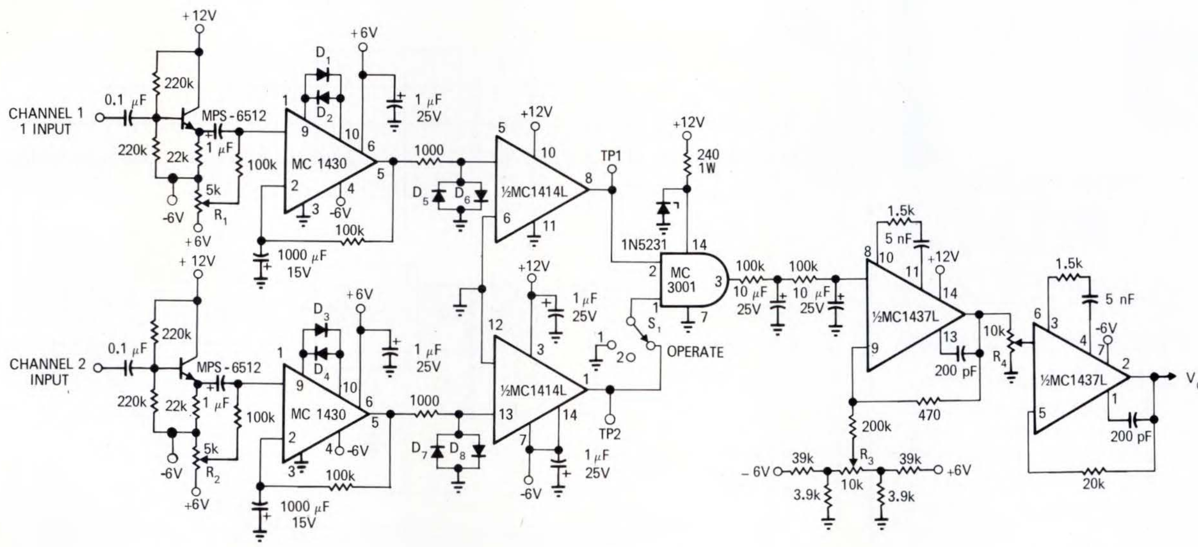


Fig. 5—**Phasemeter schematic.**

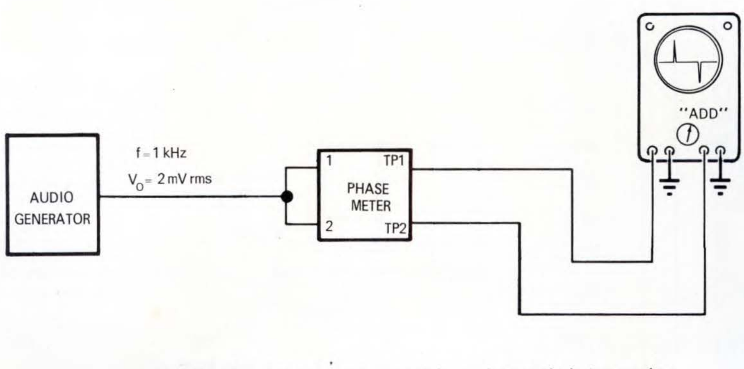


Fig. 6—**Test setup** matching channel duty cycles.

(Continued)

IC Φ Meter *(Cont'd)*

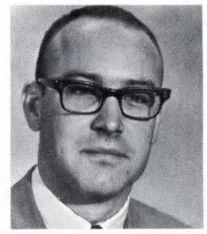
in bounds for some measurements, as illustrated by **Fig. 8**.

It is quite easy to determine the 3-dB point from the phase plot (for minimum phase networks) by locating the 45° point.

The meter's high input impedance of 100 kΩ will not load most circuits to be tested. ▭

Acknowledgement

The author wishes to thank Mike Garden whose encouragement and perseverance brought the project to a successful conclusion.



Don Kesner is a section manager in Industrial Systems at Motorola Semiconductor, Phoenix, Ariz. Kesner has been with Motorola for 5 years and was previously with Western Electric and Bell Telephone. He holds a B.S.E.E. from Kansas State University and an M.S.E. from Arizona State.

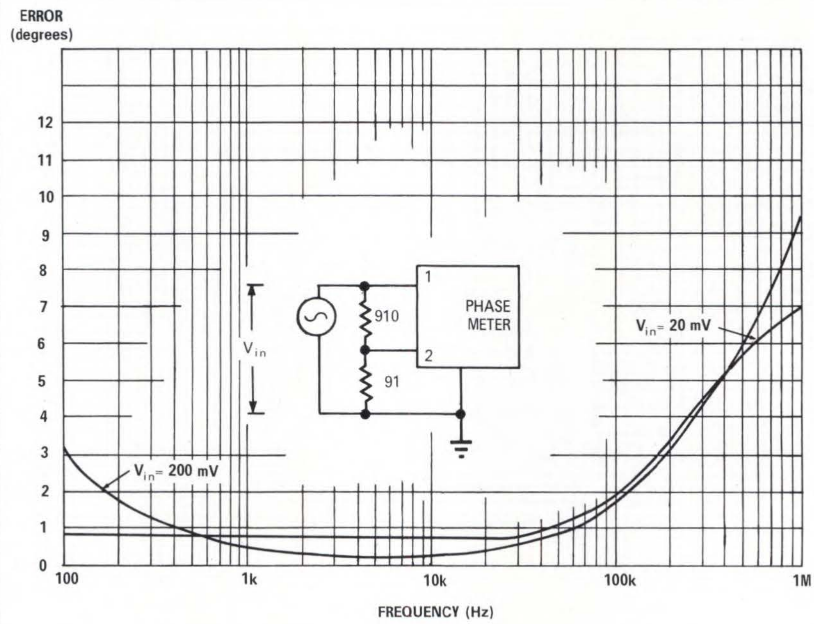


Fig. 7—**Error** for 20 dB attenuation between channels.

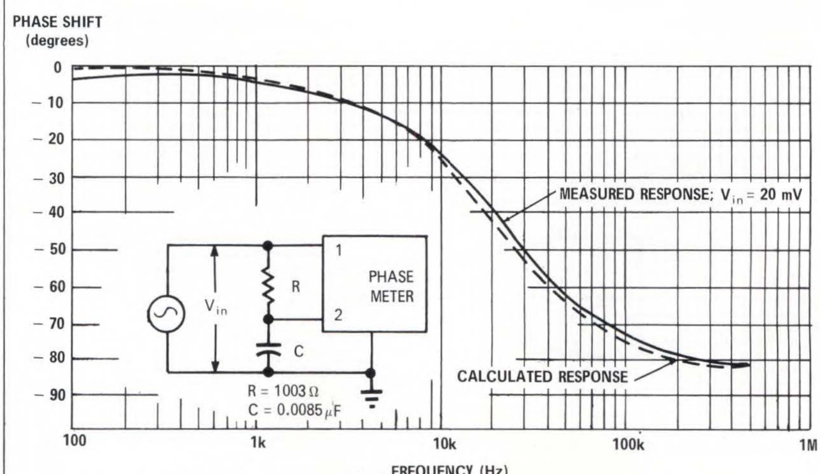


Fig. 8—**Measured phase shift** with a single-pole network.

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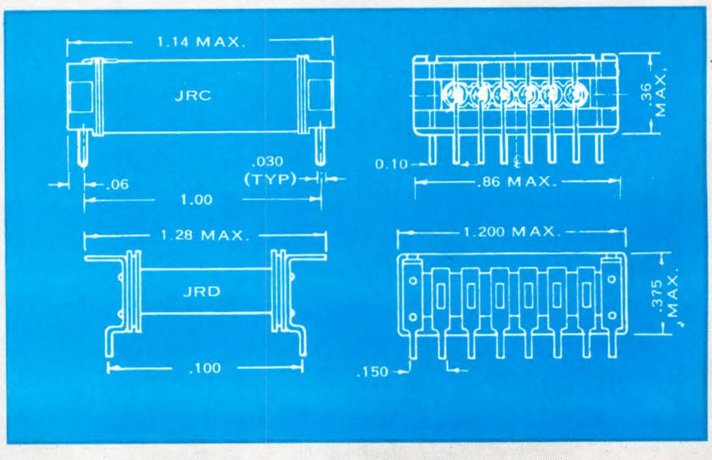

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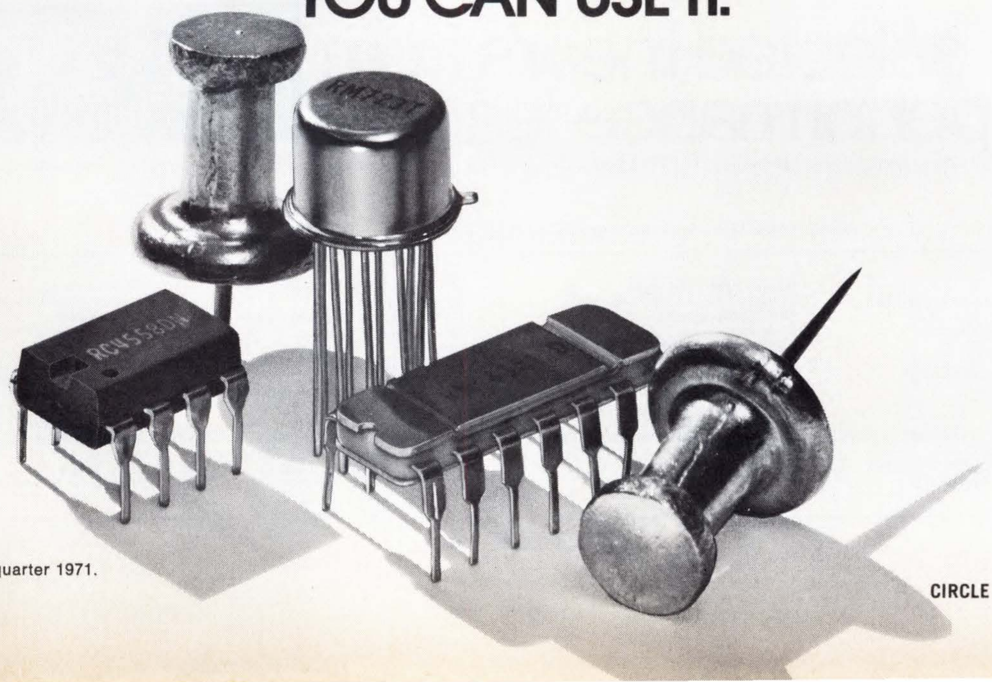

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CIRCLE NO. 30

Determining Subminiature Lamp Life

Accelerated life tests of subminiature lamps can lead to unrealistic average life ratings. Here's some good advice on pitfalls to avoid in testing, and a filament volt-ratio equation that provides realistic life values.

OTTO J. FORSBERG, Chicago Miniature Lamp Works

Life ratings of miniature and subminiature lamps are usually determined by accelerated testing at higher-than-rated voltages when life ratings exceed 5000 hours. A simple equation is then used to determine average expected life at the rated voltage. Tests show that very optimistic ratings result when the usual formula is used if there are large differences between test and rated voltages.

Converting the average hours to burnout in an accelerated life test to the average life at design voltage or any other lower applied voltage is usually done with the following formula:

$$L_{DV} = \left(\frac{V_T}{V_D}\right)^{12} \times L_{TV}$$

L_{DV} = Life in hours at design voltage.
V_T = Accelerated test voltage.
V_D = Design voltage.
L_{TV} = Life in hours at test voltage.

To test the validity of the exponent 12 in this equation, an accelerated life test on the CM-6833 lamp, rated at 5V, 0.06A in a T-3/4 bulb, was made at two different fixed voltages of 7.2 and 8.0V.

It is important in accelerated life testing to select a filament voltage such that only recrystallization and evaporation rates for the tungsten filament are increased without overheating the glass envelope with the possible initiation of the "water cycle." When that occurs, free H_2O molecules move about continuously in the vacuum and attack the filament, creating the possibility of complete burnout of all lamps in a test lot in less than 6 months or 4380 hours.

The test consisted of nine lamps each. At 8V, burnouts ranged from 546 to 2536 hours, with an average of 1692 hours. At 7.2V, burnouts ranged from 1128 hours to 7056 hours, average 3293 hours.

Using the 12th power exponent for both tests we arrive at unbelievable average life figures of over 475,000 hours from the 8V test and over 262,000 hours from the 7.2V test. These figures, 54 and 30 years respectively, are not realistic and show the runaway characteristic of this equation when used with a relatively large volt ratio.

Because of the inevitable recrystallization growth change of all tungsten filament lamps over many thousands of hours, the actual life performance falls far short of that calculated by using the 12th power formula on voltage ratio. During the many thousands of hours of incandescent operation, the long fibrous interlaced tungsten crystals gradually change into relatively short stocky crystals, forming segments throughout the length of the filament. Gradually, the interfaces of the larger crystals will extend across the body of the filament, creating cleavage regions where the filament will eventually fail upon application of some small shock force.

How can we then arrive at some meaningful value of average life performance when we derate the voltage applied to these lamps and still use the simple volt ratio method?

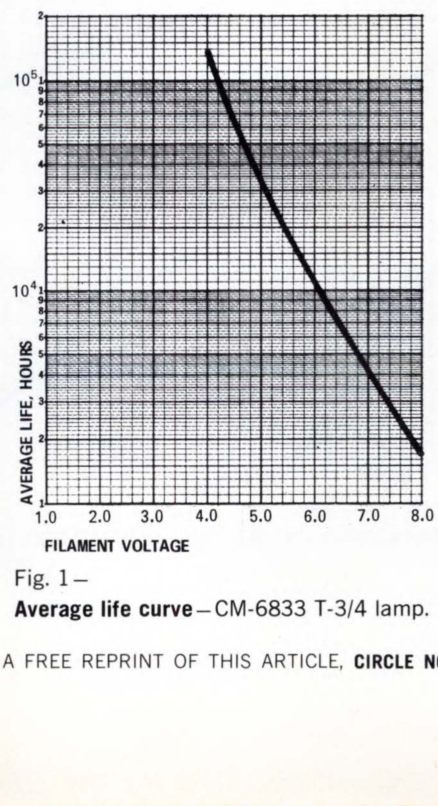

Fig. 1—
Average life curve—CM-6833 T-3/4 lamp.

Determining a New Exponent

It is logical to assume that if we were to run two or more tests as above, the resultant life (L_{DV}) should have the same or nearly the same value in hours for either volt ratio when the same exponent is used.

Therefore, we will equate both life test expressions and solve for the exponent X.

$$\left(\frac{8.0V}{5.0V}\right)^X 1692 \text{ hours} = \left(\frac{7.2V}{5.0V}\right)^X 3293 \text{ hours}$$

$$X \log 1.60 + \log 1692 = X \log 1.44 + \log 3293$$
$$0.2041X + 3.2284 = 0.1584X + 3.5176$$
$$0.0457X = 0.2892$$
$$X = 6.33$$

It is important for the exponent to be calculated to three significant figures to yield errors of less than 2% on average life calculations.

(Continued)

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Lamp Life (Cont'd)

Solving the original equation with the exponent 6.33 yields:

$$\left(\frac{8.0V}{5.0V}\right)^{6.33} 1692 \text{ hours}$$

= 33,146 hours for the 8V test

$$\left(\frac{7.2V}{5.0V}\right)^{6.33} 3293 \text{ hours}$$

= 33,128 hours for the 7.2V test

The average life performance at 5V would be 33,000 hours for this test.

To determine what the average life would be at 4.5 instead of 5V, the above equations are solved using 4.5V as V_D. Calculations yield 63,957 hours for the 8V test and 64,477 hours for the 7.2V test.

These are practical common values of approximately 64,000 hours that we can accept. They also include the fragility factor[1] of a tungsten filament after operating for many thousands of hours at incandescent temperatures.

Solving for 6V operation, which is higher than the design voltage for this lamp, we obtain 10,456 and 10,439 hours.

Fig. 1 is a graph of filament voltage vs average life for the CM-6833 lamp using the 6.33 exponent. It indicates that life performance could be extended indefinitely simply by lowering the operating voltage. Checking the curve, we find that at 4.2V the average life would be 100,000 hours. Unfortunately, there is no positive record of any miniature lamp types that have reached this value of 11.4 years of constant burning at any incandescent operating temperatures.

We have shown only one type of lamp on accelerated life test, but the same method can be used for any other type of tungsten-filament miniature lamp. Two or more tests should be made on a given type of lamp, and the proper exponent obtained using the formula given for the CM-6833 lamp.

The voltage used in the life test should be in excess of the design voltage, but as a rule not high enough to cause life values to be below 500 hours. If life tests on long life lamps are too short, erratic test results will be obtained which will give doubtful values for average life at design voltage.

Time to First Burnout

It is practically impossible to accurately determine when the first burnout or failure will occur on a given group of lamps at some specified filament voltage. However, a close approximation can be made.

In the life test of 18 CM-6833 lamps, the life span to burnout of the first lamp was 546 hours at 8V and 1128 hours at 7.2V. If we derate these two lamps to 5V using the 6.33 exponent, we have:

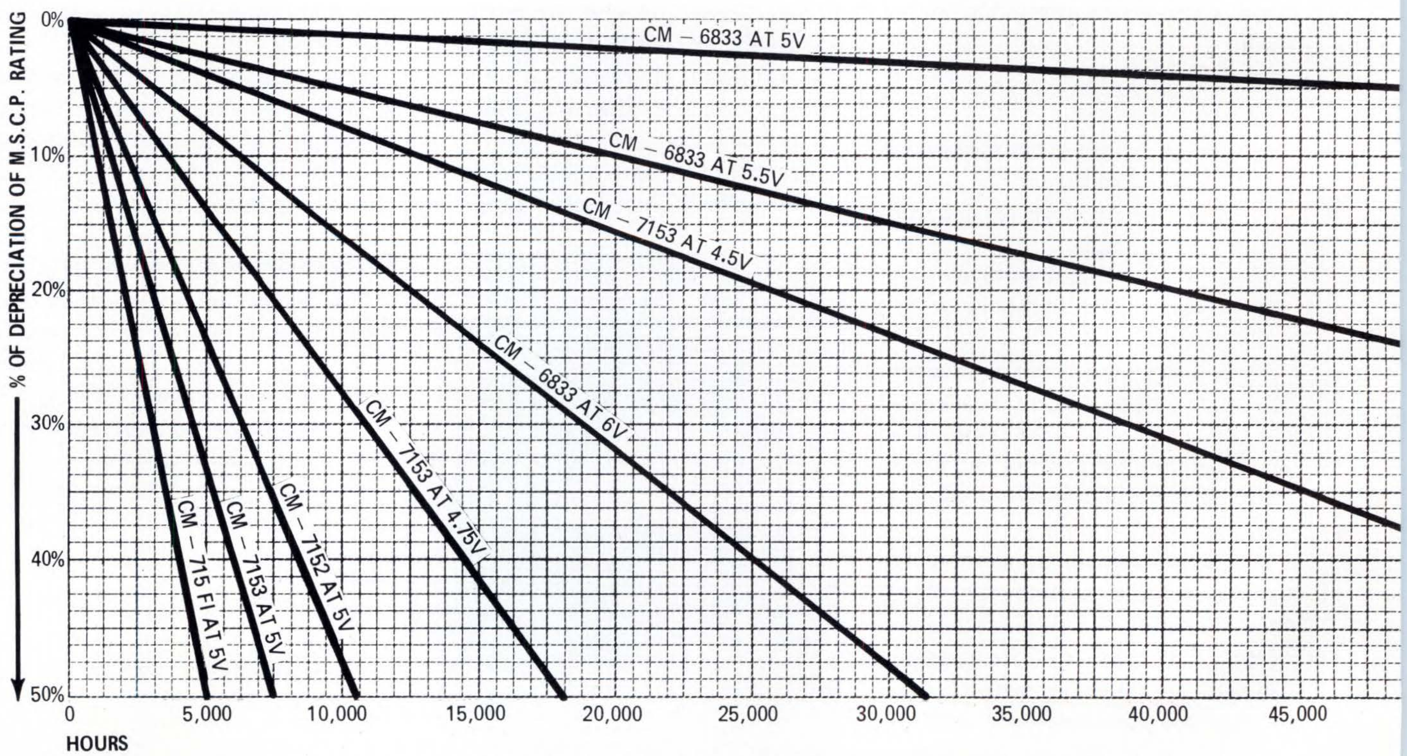

Fig. 2—**Useful life matrix.**

LAMP RATINGS BY MODEL				
MODEL	VOLTAGE	CURRENT	MSCP	BULB
CM 715FI	5V	0.125A	0.22	T-1
CM 7152	5V	0.115A	0.147	T-1
CM 6833	5V	0.060A	0.053	T-¾
CM 7153	5V	0.115A	0.147	T-¾

Table I

$$\left(\frac{8.0V}{5.0V}\right)^{6.33} 546 \text{ hours} = 10{,}702 \text{ hours at } 5V$$

$$\left(\frac{7.2V}{5.0V}\right)^{6.33} 1128 \text{ hours} = 11{,}350 \text{ hours at } 5V$$

These were aged and selected lamps that show good agreement for first burnout or failure. Bear in mind that the time to the first failure in each of these two test lots of 18 lamps does not have a definite value. If 100 lamps were life tested from this same lot, one or two lamps would probably have failed in less than 10,700 hours on 5V operation.

We can use 10,000 hours as a maximum value to first burnout for the type CM-6833 under the most favorable end-use operating conditions for clear lamps.

Where lamp confinement causes heat build-up of the glass envelope, or where the lamp is subjected to more vibration or shock due to close-in mechanical devices, the average life of these lamps as well as the time to first burnout will be less than the figures derived from the preceding test values. If these conditions will be encountered, accelerated life tests on two or more lots of lamps should be made under actual end-use conditions to arrive at a new exponent value. This value should then be used to determine average life at some lower filament voltage.

Light Output Depreciation

Failure due to burnout is not the only failure mode to be considered in life testing. There is also a measurable depreciation in light output as a function of time which provides an entirely different basis for evaluation.

Fig. 2 shows a matrix pattern of "useful life" that is used in determining the amount of mean spherical candlepower loss at a given number of operating hours for specific lamps listed in **Table I**. The diagonal lines represent the rate of depreciation and not the life-to-burnout values.

Where these small lamps are used as indicators or for localized illumination, the depreciation in light output that can be tolerated may be anywhere from 10 to 50% and depends on the end use of the different lamp types.

Summing Up

Average-life data from accelerated life tests, when calculated as described, should provide more meaningful results than those obtained using the old 12th power relationship —because the exponent used in the new volt ratio equation is derived from actual test data.

It should be remembered that useful life may be different from average life to burnout. Lamp darkening during use may reduce light output below an acceptable level before burnout occurs. □

[1]The term "fragility factor" as used here is an overall coverage of the "notching" characteristic of the filament surface as it recrystallizes after prolonged operation at temperatures used in these lamps. ("Observation of Electromigration and the Soret Effect in Tungsten" by Dennis O'Boyle, *Journal of Applied Physics*, Sept. 1965, pp. 2849-2853.)

Otto J. Forsberg, at 79 years of age, is chief design engineer with Chicago Miniature Lamp Works, Chicago, Ill., and is presently in charge of development of alphanumeric readouts. Among his many accomplishments is a 1927 invention of a device to tell utilities linemen if a cable is "live" or "dead." Undoubtedly many linemen owe their lives to this device.

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1:30 - 4:30 p.m.	Skokie, Ill.	Teletype
Tuesday, Oct. 19		
12:00 - 5:00 p.m.	Ft. Wayne, Ind.	Magnavox (Corp. Office 11 - 1:00 (Bueter Rd. 1:30 - 3:00 (Ind. Park 3:30 - 4:30
Wednesday, Oct. 20		
9:00 - 11:00 a.m.	Dayton, Ohio	NCR
Thursday, Oct. 21		
9:00 - 12:00 noon	Southfield, Mich.	Bendix
1:30 - 4:30 p.m.	Plymouth, Mich.	Burroughs
Friday, Oct. 22		
1:30 - 4:30 p.m.	Galion, Ohio	North Electric
Monday, Oct. 25		
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Tuesday, Oct. 26		
9:00 - 12:00 noon	Owego, N.Y.	IBM/Federal Systems
1:30 - 4:30 p.m.	Endicott, N.Y.	IBM
Wednesday, Oct. 27		
9:00 - 12:00 noon	Binghamton, N.Y.	General Precision/Link
Friday, Oct. 29		
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Readers have voted J. V. Sastry winner of the July 1 Savings Bond Award. His winning circuit was called "Gated Clock Generates Pulse Train or Single Pulse." Mr. Sastry was formerly with Westinghouse Electric, Pittsburgh, Pa.

Crystal-controlled relaxation oscillator

To Vote For This Circuit Circle 141

by Robert D. Clement and Ronald L. Starliper
Western Electric Co.
Burlington, N.C.

In a conventional relaxation oscillator, operating frequency is determined primarily by the circuit's RC time constant. But any variations in resistance, capacitance, ambient temperature or power-supply voltage will cause the oscillator s frequency to change.

Frequency stability of a relaxation oscillator can be improved, however, by adding a crystal in the frequency-determining circuit. Since the crystal controls oscillator frequency, the circuitry is therefore less susceptible to power-supply variations and compo-

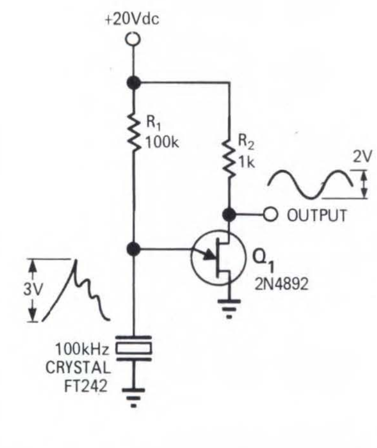


Fig. 1—**Crystal-controlled** relaxation oscillator is similar to RC oscillator except that a crystal replaces the capacitor.

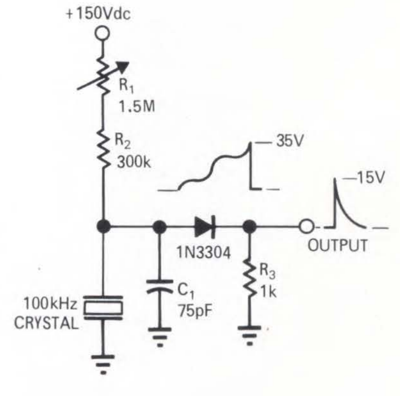


Fig. 2—**Alternative** type of relaxation oscillator uses four-layer diode. Resistor R_1 controls oscillator frequency which can be the fundamental frequency or a subharmonic of the crystal.

(Continued)

nent drift.

The circuit shown in **Fig. 1** is a fairly conventional unijunction-transistor relaxation oscillator in which the charging capacitor has been replaced by a 100-kHz quartz crystal (Texas Crystals Type FT243 or equivalent.) The output waveform at base 2 of the UJT is a distorted sine wave which is produced when the crystal capacitance discharges through the UJT. The signal at the emitter of the UJT is a damping-type discharge as shown. The circuit shown yielded a measured output frequency of 99,925 ±1 Hz. A version with a 1-MHz crystal had an output frequency of 999,663 ±1 Hz.

Another type of crystal-controlled relaxation oscillator is shown in **Fig. 2**. This version uses a four-layer diode as the active element.

Capacitor C_1 is needed across the crystal because the crystal capacitance alone cannot supply enough energy to sustain oscillation. Variable resistor R_1 allows adjustment of the RC time constant so that it is close to the crystal's resonant frequency, thus allowing the oscillator to lock to the crystal frequency. Note that this resistor can be adjusted so that oscillation occurs either at the crystal's fundamental frequency or at half the fundamental frequency.

For the circuit shown in **Fig. 2**, measured fundamental- and subharmonic-mode output frequencies were 99,934 ±1 Hz and 49,966 ±1 Hz, respectively. The output pulse appears across R_3 each time C_1 discharge through the four-layer diode. □

Digital phase-locked loop with loss-of-lock monitor

To Vote For This Circuit Circle 142

by Charles A. Herbst
Comfax Communications
Garden City, N.Y.

A phase-locked loop (PLL) can provide a convenient method of synchronizing the clock frequencies of two pieces of equipment. But this type of circuit has the disadvantage that it becomes a free-running oscillator if it goes out of lock.

The digital PLL, shown in **Fig. 1**, includes a monitor circuit. This provides an alarm, or disables other circuitry, when phase lock is lost or when the phase error between the internal clock and the external sync signal exceeds a predetermined limit.

The voltage-controlled multivibrator (VCO) in the circuit operates at four times the desired clock frequency. This VCO drives a two-stage, switch-tailed, ring counter that provides a two-phase internal clock signal.

The "B" phase of the clock is compared with the incoming sync signal in an exclusive-OR phase detector. When the two signals are locked 90° out of phase with each other, the phase detector produces a "zero" error voltage of about 2V (see **Fig. 2**) which forms the control voltage for the VCO. As the phase difference be-

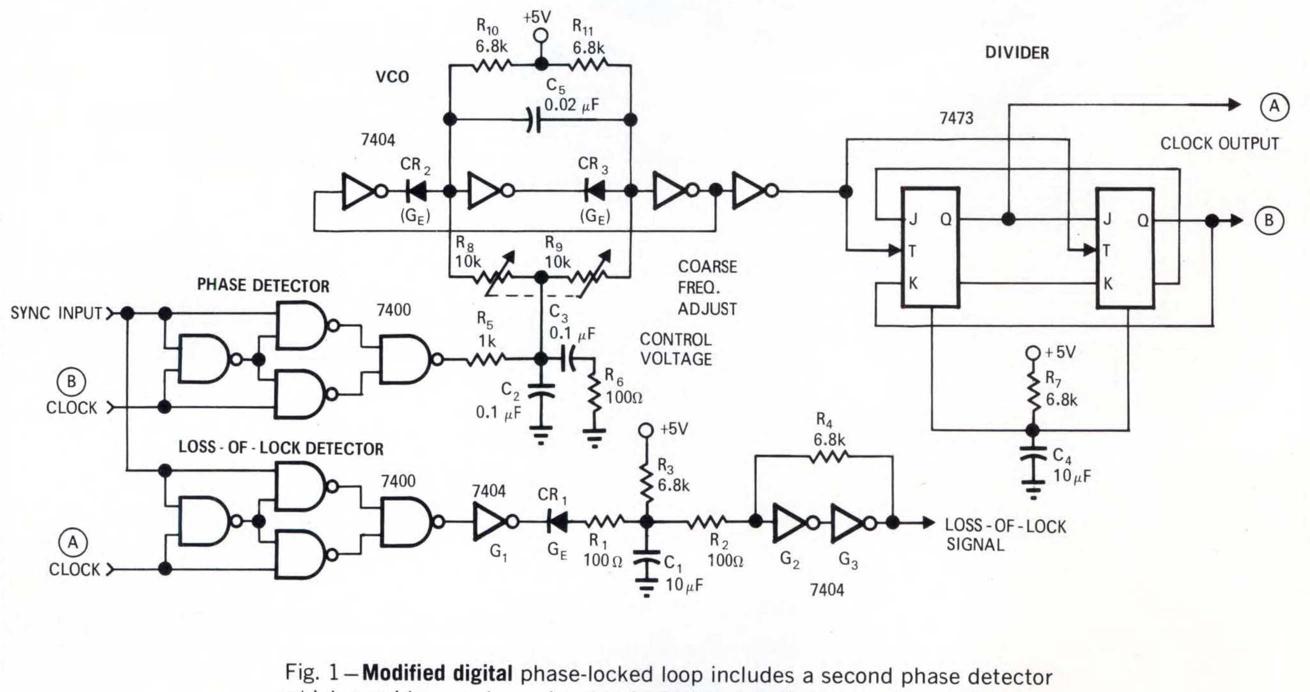


Fig. 1—**Modified digital** phase-locked loop includes a second phase detector which provides an alarm signal to indicate when the loop gets out of lock.

tween the two signals varies ±90° from the normal lock condition, the control voltage swings approximately ±2V from the "zero" value and in a direction which tends to reduce the phase error and bring the loop into lock.

A second exclusive-OR gate compares the "A" phase of the clock with the incoming signal. This "loss-of-lock" phase detector determines when the two signals are in step with each other. When they are in phase, the output of G_1 stays at a high logic level, indicating an "in-lock" condition. As the two signals begin to get out of phase with each other, small negative-going pulses (whose widths indicate the magnitude of the phase error) begin to appear at the output of G_1, causing C_1 to commence discharging through R_1 and CR_1. If the pulses get wide enough to discharge C_1 below the trigger point of the Schmitt trigger (G_2 and G_3), then an "out-of-lock" condition will be indicated. Failure of either the VCO or sync signal will also give an "out-of-lock" indication.

The network R_7 and C_4 provides a power-on clear circuit which ensures that the ring counter starts in the correct state. The network R_5, R_6, C_2 and C_3 is a low-pass filter which determines the dynamic response of the loop and removes carrier ripple from the control voltage. Capacitor C_5 sets the VCO center frequency, while C_1 sets the trigger point for the phase-error alarm. □

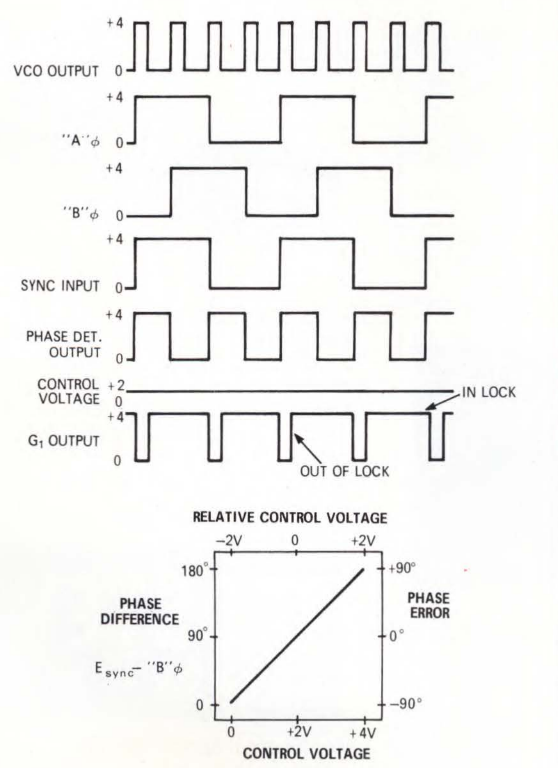
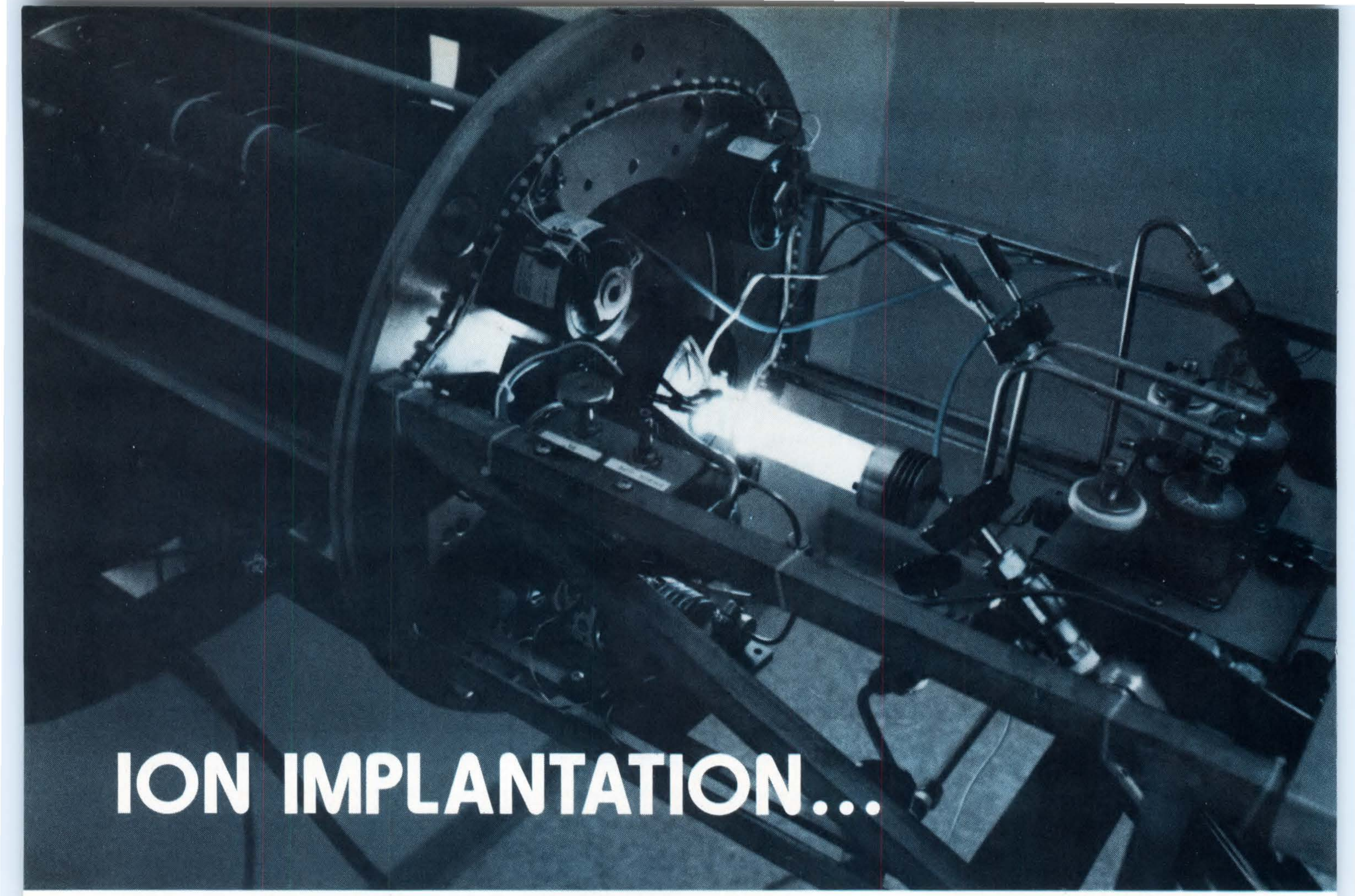


Fig. 2—**Timing diagrams** (upper) and phase-detector characteristics (lower) for the digital PLL.



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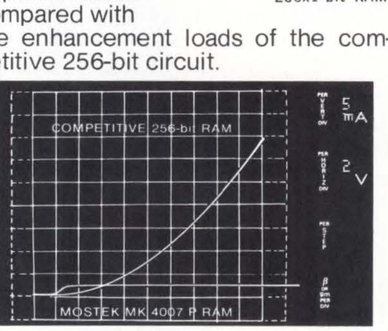
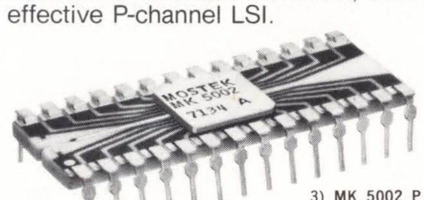


FIGURE 1

Single 5V supply operation. MOSTEK's MK 5002 P 4-digit counter/display circuit for instrumentation purposes can operate from a single +5V logic supply, drawing less than 25 mW, or from any supply from 4.5 to 20V! Ion implantation is the only processing tool capable of delivering this performance from otherwise conventional, cost-effective P-channel LSI.



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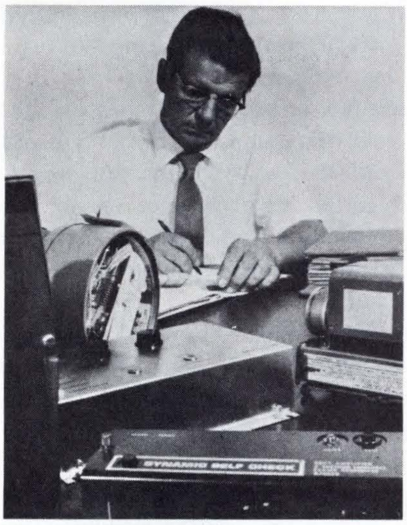

·Team design . . . Individual Responsibility

Shifting From One Industry To Another— How Transferable Is the Engineer?

The director of engineering for a large commercial division of a major company tells how five engineers fared in their transfers from different industries and different specialties to his division.

NATHANIEL ROBBINS, JR., Honeywell, Inc.

I am responsible for a 450-man engineering team. You are probably familiar with some of our products—the heating controls in your house or apartment may very well have been made by our division. Our designers have been traditionally electromechanical, but now we are also working on much more sophisticated electronic systems for the residential heating and cooling systems of the future.

My division's steady push towards broader product lines, increased product sophistication and improved product reliability has made us ever on the alert for new engineering talent. In the past few years we have taken men from both similar and different industries and from similar and different technical specialties. As the value of my operation depends on the quality of our engineers, I have followed with great personal interest the career of each man we have hired. I have been especially interested to see what factors really count.

In analyzing specific case histories—such as the five I'll be discussing—I have come to realize that it is usually the nontechnical factors that make or break a man. An engineer's technical knowledge is easy to judge in advance, but the man's work style is almost impossible to predict. I have seen evidence that it may be better to hire a man from a different industry—such as aerospace in our case—if you can predict that he has the adaptability and willingness to learn your group's ways, than to hire a man from your own industry who does not have these qualities. The catch is that it is very hard to judge these personality factors in advance.

(Continued)

Three Successful Transfers

Some of our best finds in recent years have been from the aerospace and computer industries. During the interviews, some of these men did not look too promising with respect to their understanding of our industry or our group's way of operating, but it turned out they could learn quickly.

Successful Case No. 1 was a man 27 years of age from the aerospace field who found that he not only quickly adapted to our different way of doing things, but that he liked it much better. His experience was about as far away from our business as you can get—he had been working on missile systems, establishing their aerodynamic coefficients.

The first assignment we gave him was to do an analysis of the degrees of freedom of a simple bimetal actuator that was part of a furnace safety switch. He accomplished this, and was very readily able to tell us the ranges of satisfactory performance.

His next assignment was to develop a control system for residential heating and cooling systems. This he also accomplished to our satisfaction.

Both of these assignments were somewhat related to the man's earlier aerospace work in that they involved analog and digital computer simulation and analysis. But the similarity ended right there. The cost and performance constraints on our designs were far different.

The real difference, however, was in the working environment. We don't usually put more than one engineer on most of our design and analysis tasks. Although he will have support from our drafting, modelmaking and computer groups, it is up to him to get the job done on schedule. He must interface efficiently with the support groups, giving them the direction they need to help him.

This man neither overworked the assigned problems nor underworked them. He bored right into them and produced results on schedule . . . just the sort of performance that makes an engineering manager like myself happy. I attribute this success to a good academic grounding in engineering analysis plus the fact that he could adapt quickly to our style of operation.

Successful Case No. 2 was a man of 37, with a B.S. in electrical engineering and working on his masters. He had been involved with defense and computers at both the systems and the component level. We liked the fact that he was an EE with electromechanical experience, but we did have reservations about the fact that all his experience had been on low-volume items.

His first assignment was to develop a new electromechanical control for starting an oil burner. If you own a home, you'll know this as the unit that starts your furnace, checks the flame and shuts it down if proper ignition has not occurred. This control may look simple enough to you, but if you ever had to produce it at our mass volume you'd know it can be quite a design challenge.

This man had to work very closely with the production-engineering support group to achieve the lowest

Commercial: One man responsible for many projects.

Aerospace: Team of men responsible for one system.

possible cost and the highest possible producibility. This he did and he gave us results on schedule.

He did have one thing working for him though. As a transfer from Honeywell's ordnance department, he already knew something about how our company operates. He was fully aware that he was expected to provide leadership to the production-engineering support group.

Successful Case No. 3 was more typical of the type of man we hired before the aerospace depression (back when many engineers turned up their noses at our prosaic product lines despite our truly long-term stability). This man's background almost exactly matched what we needed. He came from manufacturing, and that was where we needed him. He was familiar with the economics of our high-volume production. His academic degree was, appropriately, in mechanical engineering.

About the only things, he needed to learn were our communication and personnel procedures. These "people problems," as I have said, can be rough stumbling blocks for newcomers, but he was able to comprehend our "style" right away and immediately began to contribute.

Unsuccessful Transfers

Some of the cases where the man did not work out equally well reinforce my thesis that adaptability to work styles may be more crucial than specific technical experience. Each of the following unsuccessful examples appeared, when hired, to have ideal technical experience. Both came from commercial companies and from technical specialties either closely aligned with or identical to what they were to do with us. Yet each had difficulty in adjusting to our way of doing things.

Unsuccessful Case No. 1 came from a very similar industry—he had been designing copying and printing machines. These electromechanical devices might not have had quite the same production volume as our products, but they were basically the same technology. Moreover, this man had an excellent academic background: a B.S. in mechanical engineering topped off with a masters in math.

He was very personable, and appeared to be mature and highly motivated—the type of person who is very responsive to your questions. He was a very hard worker—the type you never find standing around in hallways.

But in the 2-1/2 years he worked with us, he never achieved the performance we expected.

Our organization, as I have said, gives each engineer sole responsibility on projects. To help him succeed, we back the man up with large, well-organized service groups like drafting, model making and testing. The individual project engineers must give clear, unambiguous direction to these support groups.

This man couldn't seem to work effectively with the support groups. He'd give them vague instructions, things would go wrong and they would have to be redone. You can imagine how this irritated the support groups and how the blame would fly back and forth. His projects would start slipping behind schedule. Little problems would build into bigger problems un-

(Continued)

til his projects became major "panics" to his superiors.

We had to let this man go.

Unsuccessful Case No. 2 was similar to No. 1. Here was a man who looked "right on" technically, yet who turned out to be "all wrong" psychologically.

We wanted to start a new product line in a type of relay we had never produced before. This man was with a competitor who had produced that type of relay. We hired this "expert" thinking he would start our relay line without any problem.

Well, things went according to schedule right up to the last moment. That the project ran into trouble wasn't in itself unusual; all engineering programs can do that. But what was wrong was the way this man tried to correct the trouble.

We tried to give him extra help from the support groups, but like the first unsuccessful man, he couldn't seem to make use of them. His former work style had been a one-man show. No doubt because of lack of such support groups, he had been forced to be designer, draftsman, model maker and test engineer all rolled into one.

You might say, why not let the guy do his own thing and operate the way he likes? That may be all right in some smaller companies or in situations where you don't have customers hollering for the product you've promised them, but it isn't enough for our organization. We can't afford the uncertainty of waiting around for a one-man show to do it all himself, especially when we've got expensive support groups who've proven they can help in such emergencies.

The upshot of this transfer was a mutual parting of the ways, and a temporary abandoning of that new product line.

Salary Picture

I don't think the salary difference among various industries is as much of a problem as it is made out to be. We have both defense and nondefense divisions at Honeywell, and the difference in engineer's salaries between these groups has not of itself been an obstacle. I think the only engineers in aerospace who were really overpaid were the extreme specialists, and in a way you can consider their high salaries compensation for the risk they took in specializing.

I feel that if a man from another industry is making 10% more than you normally pay, you should take him on anyway and hope he'll catch up. But if he is making 15% more, you might hesitate.

Conclusion: Be Sensitive to Work Style

The table summarizes how the five transfers checked out on five different factors that I judge important in hiring. Right away you'll note the danger of placing blind faith in any simple checklist. The man who checked out highest—the last man—actually was our worst choice, and the two who checked out lowest—the first two—actually were two of our best choices.

All of this points up a valuable lesson for ex-aerospace engineers (and conversely for engineering managers). Be very sensitive to the work styles of companies. Try to learn in advance what the work style is and to consider whether or not you will like it. ▭

Nathaniel Robbins has been director of engineering for Honeywell's Residential Division, Minneapolis, Minn., for the past 9 years. This division, which specializes in "home comfort controls," is very definitely nonmilitary. But in his 23 years with Honeywell, he put in 6 years with the Aerospace and Ordnance divisions, so he knows "that side of the fence" also.

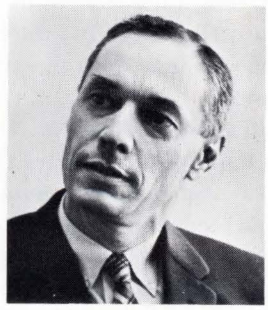

TABLE 1-FACTORS vs CASE HISTORIES

FACTOR	TRANSFER CASES				
	SUCCESSFUL			UNSUCCESSFUL	
	No. 1	No. 2	No. 3	No. 1	No. 2
1. SIMILAR EXPERIENCE?	No	No	Yes	Yes	Yes
2. APPLICABLE ACADEMIC BACKGROUND?	Yes	No	Yes	Yes	Yes
3. FAMILIARITY WITH WORK STYLE?	No	Yes	No	No	No
4. KNOWLEDGE OF MARKETS AND CUSTOMERS?	No	No	Yes	No	Yes
5. ADAPTABILITY AND WILLINGNESS TO LEARN?	Yes	Yes	Yes	No	No

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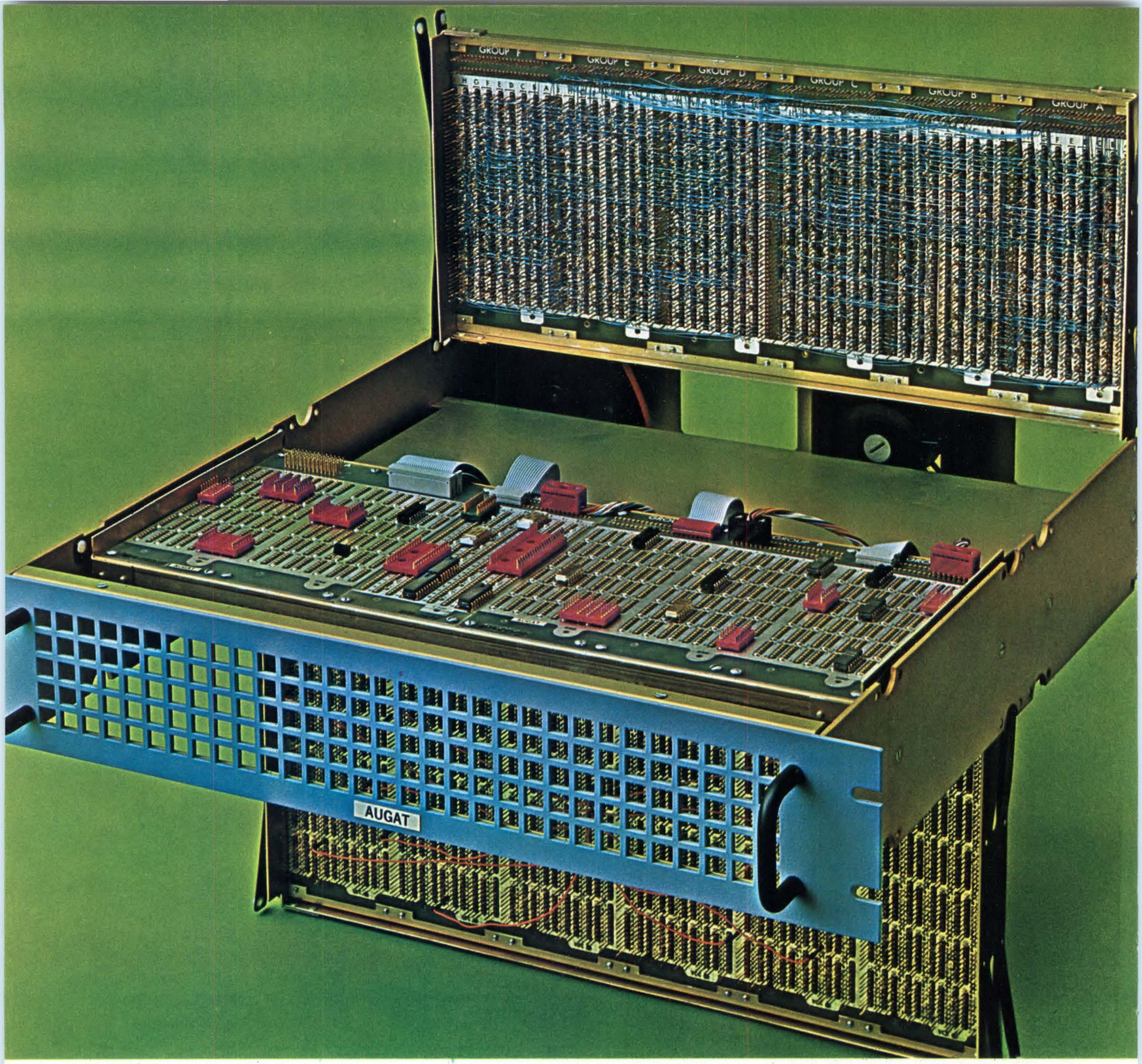

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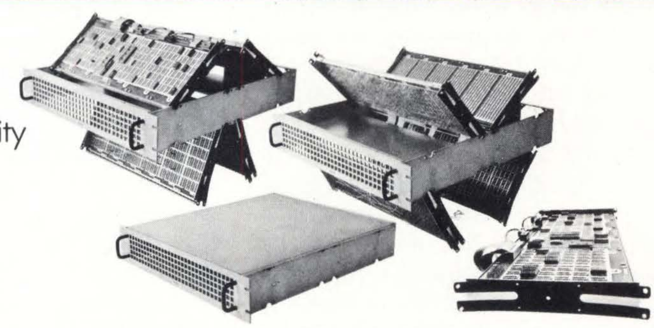

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cover

Cover by Ray Lewis, EDN/EEE Art Director, depicts semiconductor memory tester at Monolithic Systems, Inc. Just as important to memory design is "refresh." See article on page CH 13.

directions

DOT gets lift from Navy .... CH 7

DEC announces large computer systems . . . sculpture by computer . . . computer in bond . . . hot typing head speeds computer printout . . . first magnetics, then semiconductors—now ceramics . . . new company looks at $100 million market . . . computer terminal "speaks" Braille

features

"refresh" is simpler than it appears .... CH 13

Semiconductor memories consisting of dynamic storage elements offer the most advantages in size, cost and power. In order to take advantage of these memories, the refresh requirement must be dealt with.

commutating filter separates valid data from noise .... CH 17

Here is a design that not only discriminates between low baud signals with differing data rates, but is also conservative in both size and power—an advantage over the narrowband crystal filter.

push, click click—BCD .... CH 22

Digital-to-BCD conversion within keyboard design is achieved by many techniques. The unique design described in this article uses no electronic circuitry or power source.

events

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coming soon .... CH 27

coming courses .... CH 28

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feature products

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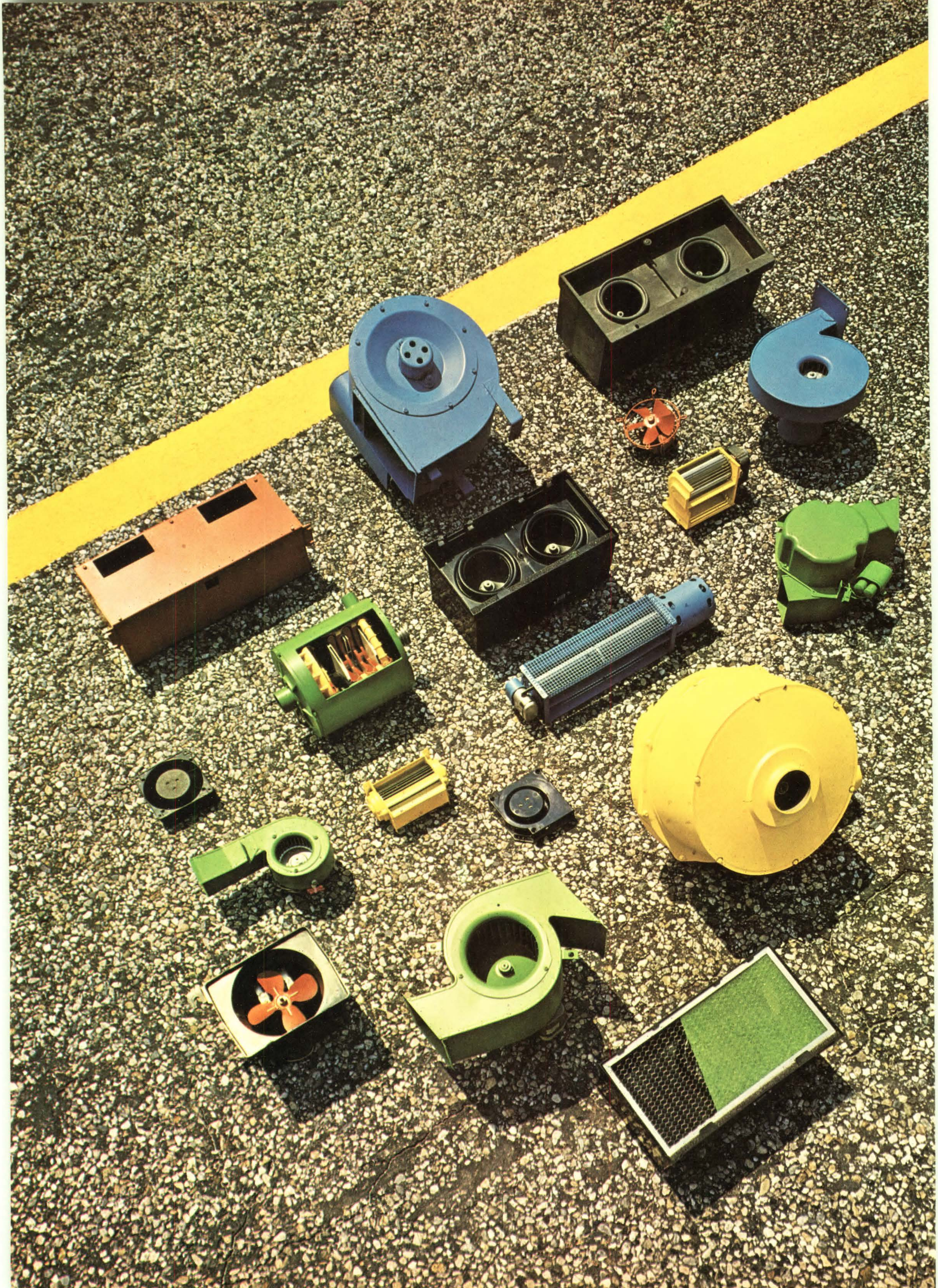

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12 Magnitron tube cooling – Crossflo® blower.
13 Contamination control disc drive – centrifugal blower.
14 Microfiche cooler – self-transition tube axial.
15 Disc Drive cooling – dual outlet centrifugal.
16 Particulate collector facsimile transmitter – ultra thin centrifugal.
17 Vacuum paper holdown – backward curved four stage unit.
18 Processing unit cooler – backward curved centrifugal.

CIRCLE NO. 404

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Canada: Oakville, Ont.
England: Swindon, Wilts.
Belgium: Nivelles
Australia: Sydney

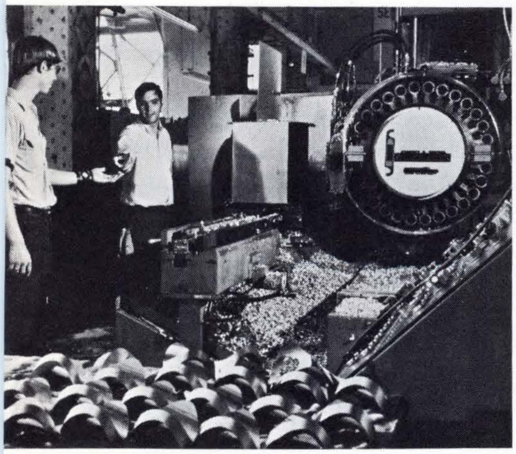
DOT gets lift from Navy—

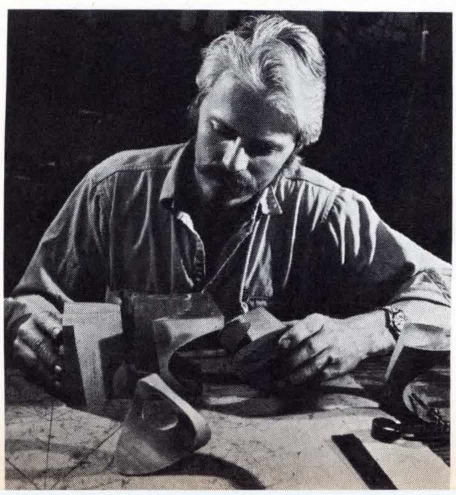
DOT (magnetic domain tip) technology (EDN Nov. 15, 1970, p. 35) has moved another step closer to reality as a rugged nonrotating mass storage system with the recent award of a $95,000 Navy contract. The Navy wants a low-cost, highly reliable, block-oriented RAM developed for future use aboard various warships and aircraft. The contract calls for two 16-bit 2k systems to be delivered to the Naval Air Development Center, Johnsville, Pa., by mid 1972. As reported in EDN, DOT is well suited for design specifications which call for the memory system to be insensitive to shock and vibration, to be nonvolatile and NDRO and to be compact and lightweight. The ultimate goal is a nonmoving mass memory capable of storing millions of bits at $0.01 to $0.03 per bit.

DEC announces large computer systems—

In a move to enhance its large computer systems image, Digital Equipment Corporation introduced five new major large scale computer systems called the DEC system-10 family. Based on its PDP-10 line, the system has a new memory, high-speed swap drums and software that provide a virtual memory system, multi-processor configurations and multi-computer networks that include DEC's minicomputers. The new systems are claimed to be the only ones in the industry that provide real-time, batch, remote-batch and timesharing capabilities under one operating system and using a single command language. The systems offer all languages and are hardware and software compatible so that users can readily upgrade their systems as the need arises.

sculpture by computer—





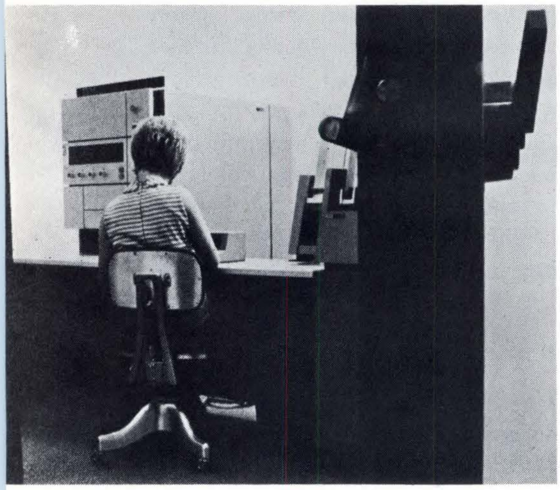
Victor Pickett, sculptor and Associate Professor of Art at a Virginia university, teamed with a computer to produce 1000 sculptures for an advertising campaign. Charles B. Clark, Art Director for Lawler Ballard Little advertising agency in Norfolk, conceived the idea and commissioned Pickett. One thousand of the computer-duplicated pieces will be mailed to chief executives of leading American corporations.

The computer sculpting plays a key role in a national campaign undertaken by Lawler Ballard Little to attract new industries to Virginia. The agency and its client, the Virginia State Division of Industrial Development, feel that the space-age art piece conveys their message well. Mr. Pickett enthusiastically agreed that it would represent Virginia as a state which combines craftsmanship and advanced technology.

Technical assistance and production support were lent by Newport News Shipbuilding. In full swing, their tape-controlled Milwaukee-Matic IIs were producing one sculpture every four minutes. The machines were programmed in APT (Automatic Programming for Tools) language and reproduced the sculpture from an aluminum cube by metal removal.

Technically described, the sculpture is "a cylinder 3-1/2 inches in diameter cut by two solid parabolas, the formula being $Y^2 = 2.30X$. The axial plane of the one parabola is tilted 6° and its origin displaced 0.50 inch to the cylinder's axis. The other parabola is tilted 10° and its origin displaced 0.07 inch to the cylinder's axis, also rotated 72° opposed to and with its origin extended into the first parabola by approximately 0.22 inch."

computer in bond—



When the Meinecke-Johnson Construction Co., Fargo, N.D., decided to install an IBM System/3 Model 10 last December, the only space available was a 12 by 14 ft fireproof vault. After redocorating, carpeting and installing air conditioning, the computer and operator were moved into their new quarters.

Dennis Olson, secretary of Meinecke-Johnson, commented, "A large general contractor may have as many as 200 labor codes representing the variety of work categories on a number of construction projects. The computer simplifies the job of classifying and summarizing these codes and their entries to provide data on actual and projected costs of a project."

"Although we weren't thinking of record security at the time," Mr. Olson said, "the room serves that purpose well. I have a secure feeling when I shut the door at night, and I don't worry about fire or theft."

hot typing head speeds computer printout—

Low noise level and 300 words a minute are the major advantages of NCR's new 260 data terminal. By eliminating the conventional ink-and-impact printout concept, NCR has made a significant reduction in ambient noise that should be welcome in computer rooms.

In place of type heads, the 260 uses a 5 × 7 dot matrix of heating elements. Cycle time of these heaters is 10 msec (cold-hot-cold) per character and printouts are achieved at a 40 msec per character average.

The 5 × 7 dot configuration prints two font sizes, simulating upper and lower case. In conjunction with NCR thermochromic-dye paper, the printhead produces blue characters on a background of any of eight colors, including white. The NCR 260 is compatible with ASCII, Baudot or CCITT codes.

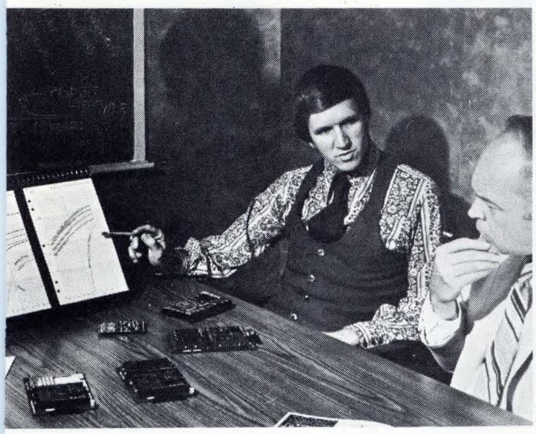
first magnetics, then semiconductors—now ceramics

One square inch of a ceramic material, developed by Honeywell Ceramics Center in Golden Valley, Minn., conceivably could hold a 2-million-bit computer memory. This 0.005-inch-thick chip could also be a picture tube for a miniature color TV.

"New ceramic materials with unique electromechanical and electro-optical properties are finding numerous applications in advanced electronic systems," said John Huff, manager of the Ceramics Center. Chips from Honeywell are currently being used in experiments at Bell Telephone, Sandia, Sylvania and Westinghouse research laboratories.

According to Clyde A. Parton, vice president and general manager of the Government and Aeronautical Products Div., industry records show that total U.S. ceramic production has doubled in the past 5 years—from $1.3 to $2.6 billion. The section that Honeywell is concerned with is a $40-million market.

new company looks at $100-million market—



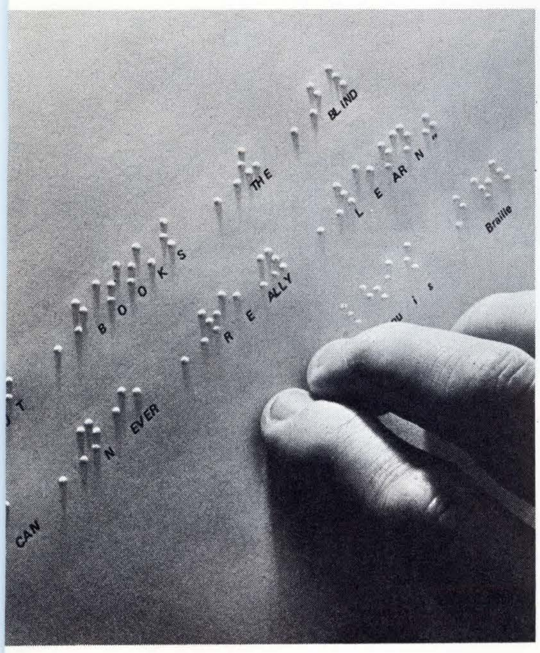
Xincom Corp. a fledgling company in Chatsworth, California, hopes to grab a hitherto unexploited segment of the $1.5 billion computer-instrumentation market. The company sees a virtually untapped market vein which lies in between the market now served by low-cost module manufacturers on one side and lab-type instrumentation companies on the other side.

Brian Sear, Xincom's president, expects this market gap to be filled by what he calls "maxi modules and mini instruments." He estimates that the market for this type of product will grow to over $100 million within the next five years.

Though Xincom's proposed packaging approach is modular, most of the company's products will have either greater complexity or better performance than existing low-cost modules. Thus the new modules will offer performance hitherto available only from expensive and bulky laboratory-quality instruments. According to Sear, Xincom's products will sell at prices in the $100 to $800 range.

Sear downplays possible competitive threats to his company's attempt to grab this market. He says "Potential competition is still very much entrenched in the basic standard laboratory instrument approach, and in many cases the products are not easily interfaceable with the latest computer technology. Special systems companies are not experienced in the engineering discipline required to develop and market standard products. And existing module companies are targeting OEM sales with low cost/complexity products which have a low margin and short life cycle. We believe that by the time these potential areas of competition become acutely aware of these problems, Xincom will have several hundred standard products which should keep us well in front."

computer terminal "speaks" Braille—



Computer terminals that converse in Braille may hold the key to an expanded world of learning and job opportunities for the blind. This idea is the basis of a study being conducted by Norman C. Loeber, an IBM engineer with an interest in putting computers to work for the blind as well as the sighted. A user enters his requests using a standard keyboard and recieves his answers in the raised-dot language of Braille at a special terminal printer.

According to Loeber, some 400 blind computer programmers in the U.S. could be the first to profit. Like their sighted colleagues, they would be able to analyze and debug programs faster through real-time communications with a computer.

More important, Loeber feels, is the terminal's potential to take the frustration out of learning for the blind school child. Today, few parents can afford the cost or space at home for even an abridged dictionary that, in Braille, fills 36 volumes and several library shelves. For these children, remote access to computerized libraries means more time to learn and less time seeking Braille reference works for help on homework assignments.

In addition, a system of this type offers the possibility of bringing "dial-up" daily news bulletins and other specialized services into the home over telephone lines—providing the blind with still another communications link with the sighted.

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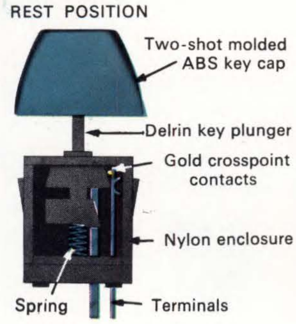

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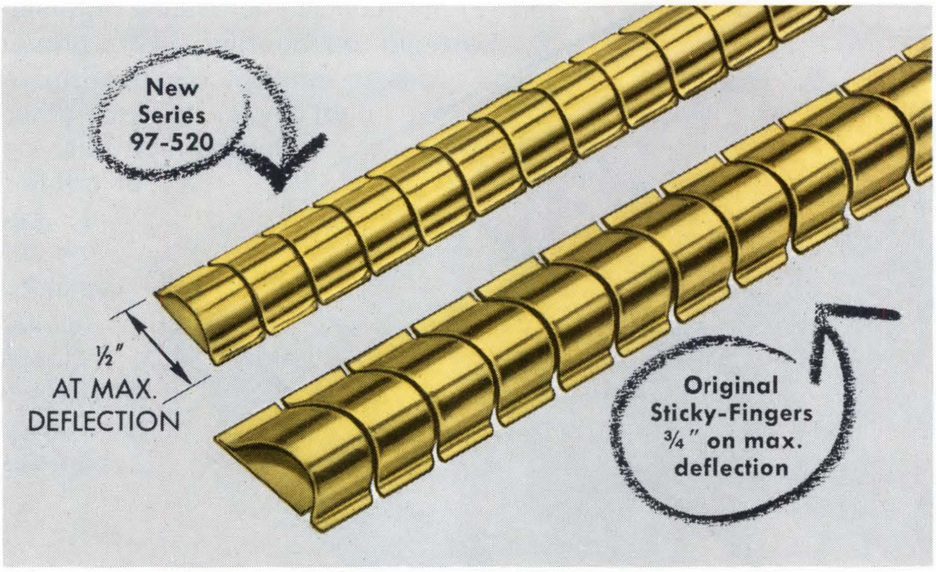

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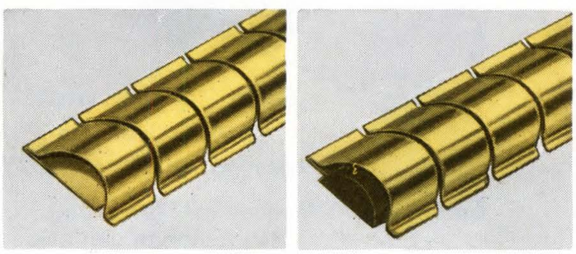

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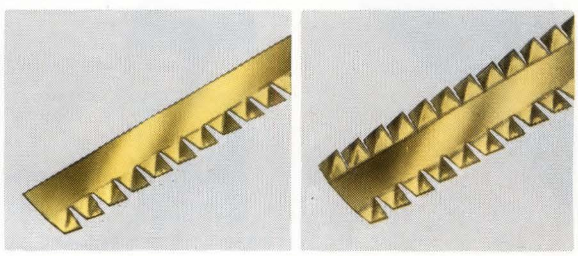

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CIRCLE NO. 407

'refresh' is simpler than it appears

Volatility and refresh requirements of the dynamic storage cell are two characteristics that make semiconductors significantly different from their magnetic counterparts. Volatility designers have learned to live with, but the best approach for refreshing remains a subject of varied opinions.

Designing a semiconductor memory into production equipment is becoming a common occurrence which continues to gain ground on other technologies. Various advantages of these memories are becoming apparent. For example, they are now almost cost-competitive for capacities up to 500k bits. Physical size is another factor. Size reduction for a semiconductor memory is at least a factor of 2, compared to their magnetic counterparts. In addition, power dissipation, reduced by one-half, provides another reduction in system size by a factor of 1.5 because of smaller power supplies. Besides cost and size, speed and performance are characteristics that are motivating designers toward the use of semiconductor memories.

For all practical purposes, the interfacing of semiconductor memories to the outside world is identical to the systems comprised of square-loop magnetic materials. However, two factors are considered to be significantly different and command special attention: volatility and refresh requirements of the dynamic storage cells. Volatility seems to be more or less accepted. Dynamic elements present the most advantages in size, cost and power. Therefore, the refresh requirement must be dealt with.

Why Refresh? Refresh requirements exist because the dynamic cell uses the substrate capacitance as the storage medium. Charge on this capacitance defines either a "1" or a "0." After a write operation, the charge begins to leak through a high impedance. The

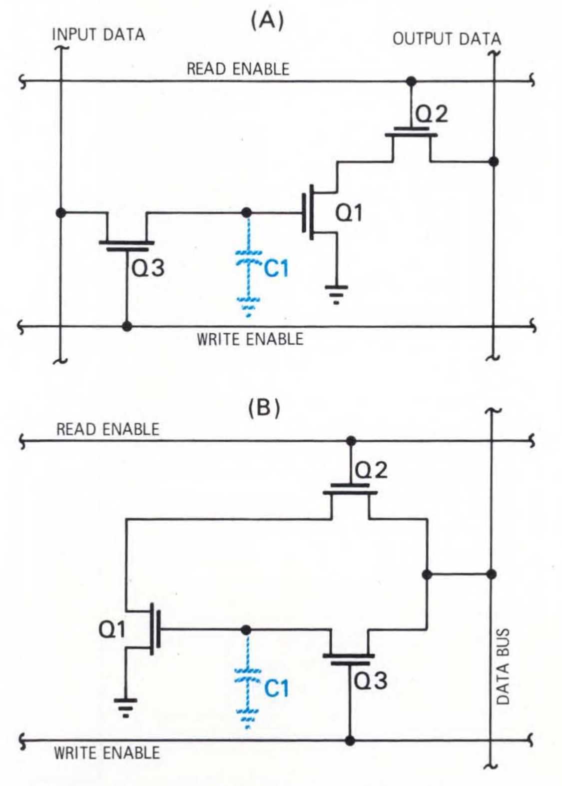

Fig. 1—**Three-transistor** dynamic cell makes use of a parasitic capacitance to hold data. Configuration **(A)** has separate input and output data lines and **(B)** has common input and output data bus.

(Continued)

FOR A FREE REPRINT OF THIS ARTICLE **CIRCLE NO. 480** discharge rate is such that the cell must be rewritten or refreshed at least every 2 msec.

The chip designer initially defines the refresh requirement. A popular concept is dividing the cells to be refreshed into 32 different groups, addressable by the five lower-order bits. The requirement is that all 32 locations must be activated at least once every 2 msec or less.

Dynamic Memory Cell. A memory element of the dynamic storage type requires less silicon area, and in most configurations, it is less complex to process. Available cells range in area from 2 to 10 square mils, compared with 30 square mils minimum for a static cell. Numerous arrangements have been described, but the most prevalent is the simple three-MOS transistor configuration.

Presently, there are two concepts of the three-transistor cell, shown in **Fig. 1**. Both configurations operate on the same principle—absence or presence of a charge on the parasitic capacitor represents the stored bit. To write, the desired data level is applied to the **input data** line and the **write** line is activated, making Q3 conduct. Capacitor C1, connected to the **input data** line, assumes a charged condition, dependent upon the state of the **input data** line. When the **write** line is deactivated, the capacitor C1 holds the data in the form of a charged or uncharged condition.

When the **read** line is activated, Q1 is connected to the **data output** line through Q2 and data is read from the storage cell. Whereas C1 establishes the state of Q1, the **data output** line will either be connected to ground or appear to be open. The status of this line represents the data bit.

There is a leakage discharge associated with the parasitic capacitor and the substrate. Characteristics of this discharge and associated circuitry gain require the capacitor to be recharged at least once every 2 msec

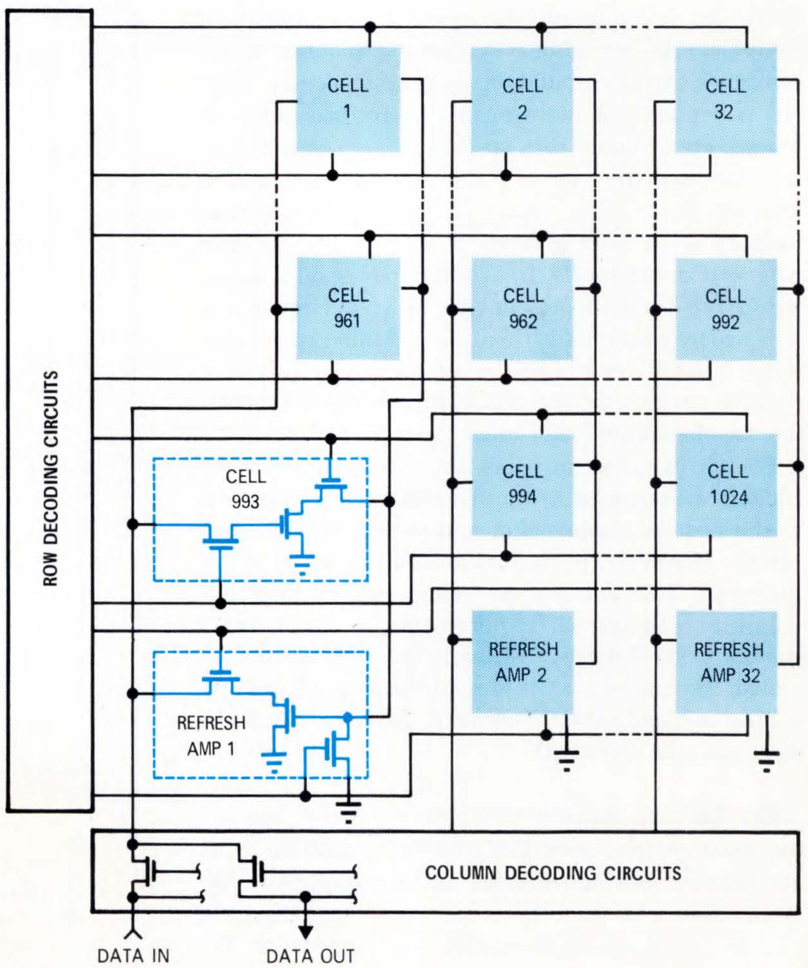

Fig. 2—**Basic cell** arranged in a matrix form.

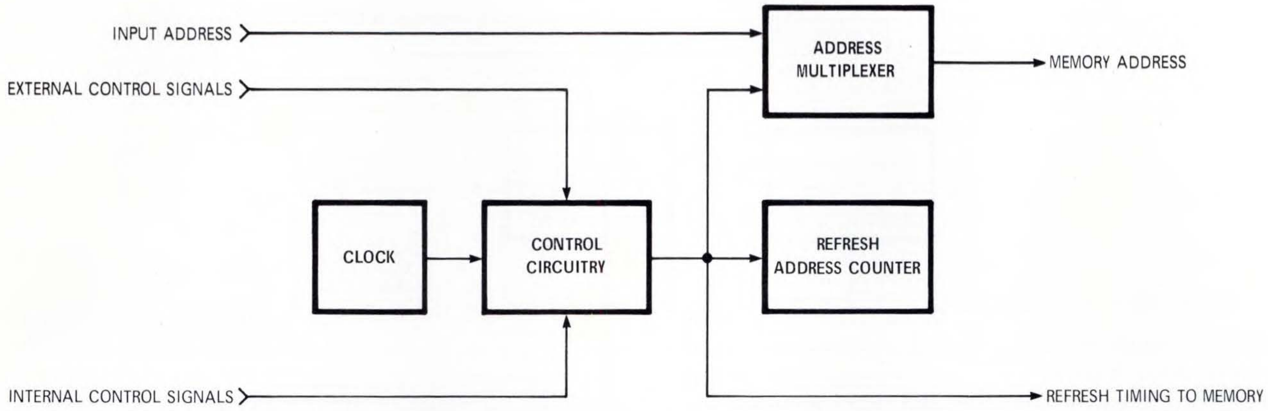

Fig. 3—**Block diagram** illustrates basic arrangement for refreshing a dynamic memory.

—basic *refresh* requirement for a dynamic memory.

Dynamic Memory Arrays. The basic storage cells are arranged in a matrix form as illustrated in **Fig. 2**. Presently, the popular organization is a 1024-bit chip arranged in a 32 x 32 matrix with row and column lines interconnecting the cells. The column lines represent the **data input/output** lines and the row lines are the **read** and **write.** Data is entered into the memory by decoding the row and column lines with a *write* enable. Data is read out of any cell by selecting a row and a column with a *read* enable. The data, on the column line, is connected to the output line through a sense amplifier and associated decoding circuitry.

With this matrix arrangement, a refresh operation is initiated with a readout by row decoding. Consequently, 32 cells insert information onto 32-column lines. The refresh amplifiers (32) invert this information and apply the results to the 32 cells associated with the enabled row. A write command re-enters the information, thus 32 cells are refreshed simultaneously. The matrix is cycled through the refresh operations under control of the five least-significant bits (LSBs) of the address word. This arrangement represents the basis for the address-oriented refresh requirements of a dynamic cell memory array.

Timing Consideration. Timing characteristics for refreshing a chip become very important when used in a memory system. Timing can be considered in two categories—the timing required for a refresh cycle on a specific location and the refresh period or time between refresh cycles. All chips have a refresh cycle that permits the chips to be refreshed in a parallel operation. However, it is also important to consider the refresh action (if any) during a read or write operation. For example, Intel's 1103 refreshes the selected chip during a read or write cycle. The unselected chips are not refreshed. For a serial refresh, this limits the array size that can be used.

On the other hand, a device such as the Mostek 4006 refreshes both selected and unselected chips on a write operation only, but not during a read. In both the Intel 1103 and Mostek 4006 refresh is address dependent. In Electronic Array's EA1500 the refresh also occurs only as a write cycle operation, but it is not address dependent. One refresh cycle on the EA1500 will refresh the entire array.

System Refresh. Design in regard to the refresh requirement of a system depends almost entirely on the application. Basic techniques fall into one of four categories—serial, cycle steal, burst and hybrid. The block diagram in **Fig. 3** illustrates the required circuitry for building nearly all refresh schemes.

Serial Refresh. Using a serial refresh depends entirely upon the application. The application must have serial addressing and the address cycle time must meet the chip refresh requirements. For example, if the address cycle time is 60 μsec, the five LSBs of the address can be scanned in 1.92 msec—time enough to refresh 1k words using the Intel 1103. Again, the chip operation influences the allowable storage capacity. With proper chip and associated circuits and an address change rate of less than 60 μsec, almost any storage capacity is possible.

Cycle Steal Refresh. This mode is the most versatile. It provides an interface timing that appears like a

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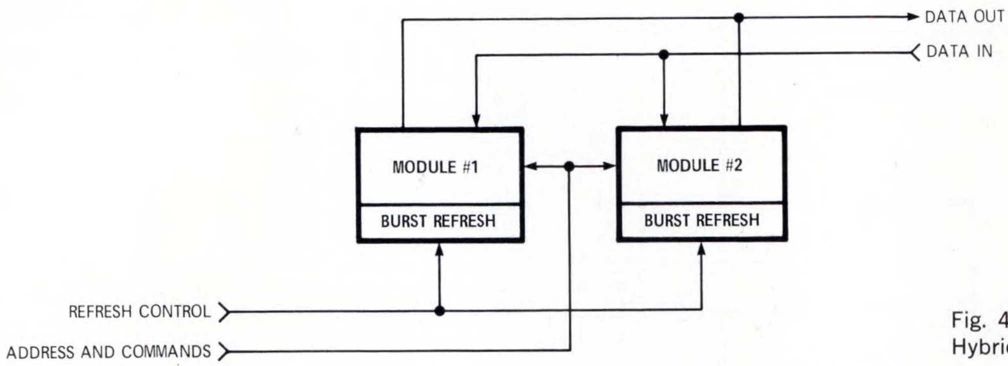


Fig. 4—**Block diagram** indicates Hybrid Refresh scheme.

static cell if the available data and cycle complete time are set to include a refresh cycle. However, if the element is to be employed at nearly its full speed capability, the stolen cycle will present a periodic delay in the access and cycle time. In asynchronous operation where the system operates on a request response basis, there are no problems. The equipment merely pauses for an extended data available and cycle complete function periodically. If this pause presents a timing problem between the input and output, another method will have to be used.

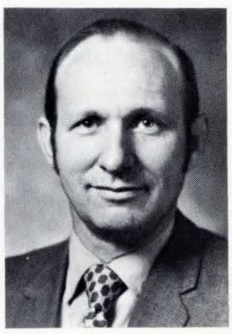
Circuitry for the cycle steal mode consists of a timing oscillator, address counter, address multiplexer and refresh timing logic. The oscillator generates a timing pulse every 55 μsec. This pulse initiates the refresh cycle if the memory is inactive. If the memory is accessed during the refresh cycle, the request is accepted and processed upon completion of the refresh cycle. The equipment making the request must wait until it receives a *delayed data available* signal. If a read operation was requested, this delay will equal the memory access time plus the refresh cycle time. For a write operation, the delay is memory cycle time plus refresh cycle time. In the event that the system operating the memory has a clock cycle, an interrupt or a delayed time period can be conveniently accommodated and the request for a refresh cycle is treated as an interrupt or a specific clock interval. This mode can provide refresh under processor control.

Burst Refresh. This approach is useful where the memory operates with a high-speed device at full speed and random addressing for a time period not to exceed 2 msec. The memory then switches to burst refresh and 32 cycles or more are performed. Then the memory is returned to service the device. This method is favorable for high-speed data acquisition applications that require the full speed of the memory and random access operation.

Hybrid Refresh. By using a combination of serial, cycle steal and burst refresh in single and multiple system arrangements, more powerful forms of refresh may be constructed. The characteristics of these systems are again mainly influenced by the application. Presently available arrangements allow no refresh delay for normal computer operation with random addressing. Systems for use with high-speed data acquisition combine multiple modules, serial operation and burst refresh. The result is MOS dynamic cell systems with 125 nsec access and 200 nsec cycle times.

In Conclusion. Dynamic cell provides the semiconductor manufacturers with the necessary storage element to develop competitive memory systems. In using the dynamic cell, the refresh requirement has been a challenge left for the memory system designer and user to solve. Arrangement of chip arrays and the timing requirements for refreshing the chip are important considerations in chip selection. Also the arrangement of the circuitry for the memory interface offers numerous refresh techniques in system application.

Hugh DeVries, one of the founders and vice president of engineering of Monolithic Systems Corp., Denver, Colo., previously was chief engineer for the Denver Systems Div. of Ferroxcube where he directed memory and computer system design. DeVries received his B.S.E.E. from the University of Nebraska. He has two patents pending and is a member of IEEE.



FOR A FREE REPRINT OF THIS ARTICLE **CIRCLE NO. 480**

commutating filter separates valid data from noise

To discriminate between low-baud signals whose baud rates differ slightly, a narrowband crystal filter may be sufficient—if size is unimportant. However, from the standpoint of both power and size, a commutating filter may be a better answer.

A digital communication receiver must detect the information bearing wave-train and simultaneously reject all spurious signals. Also, the detecting device should discriminate between signals arriving at the data rate and those with a baud rate that is slightly different from the desired rate. A narrowband crystal filter accomplishes this. At low baud rates, however, the device can be bulky—a big disadvantage if size is important. Another approach employs a commutating type filter designed with low-power complementary symmetry metal-oxide semiconductors (COS/MOS).

One such filter, shown in **Fig. 1**, sequentially switches 3-section RC networks into the circuit to produce a sharply tuned bandpass response. The switching rate determines the center frequency for the filter, and the RC networks determine the filter bandwidth and

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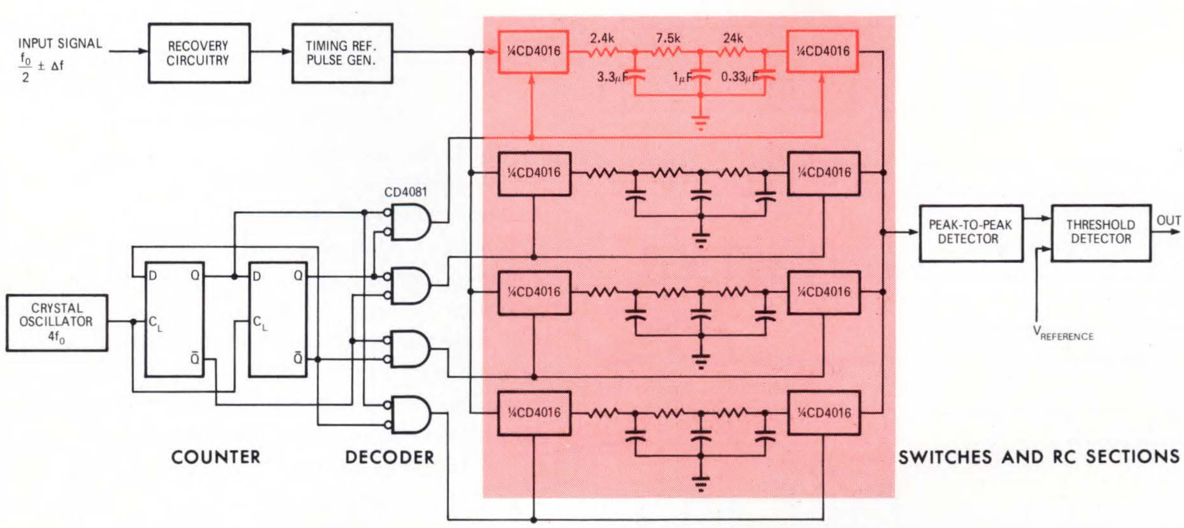

Fig. 1—**Commutating filter system** has a 20 kHz center frequency with a 3-dB bandwidth of 7 Hz for periodic input signal, 5 Hz for random. Attack time is 20 msec and dropout time is 100 msec. System logic was built with RCA COS/MOS devices. This system is actually functioning in a digital receiver.

(Continued)

rolloff. Thus, the transfer function of this commutating filter has the form:

$$G(j\omega) = \frac{\sin^2 \frac{\pi}{N}}{\left(\frac{\pi}{N}\right)^2} \left[H(j\omega - j\omega_0) + H(j\omega + j\omega_0) \right]$$

where N = number of Networks
ω_0 = switching frequency

This transfer function indicates a lowpass-to-bandpass transformation with the midband frequency ω_0 depending solely on the switching frequency. The selectivity, like the bandwidth of the filter, is determined by the lowpass network transfer function $H(j\omega)$.

A Working System. The system in **Fig. 1** uses a stable square-wave crystal oscillator operating at $4f_0$ for the local clock. The output from the oscillator drives a counter comprised of two flip-flops (CD4003). A set of NOR gates (CD4001) decodes the flip-flop outputs to produce four sequential switching pulses.

A binary input signal at a frequency of $f_0/2$ first passes through a recovery circuit that detects the bits

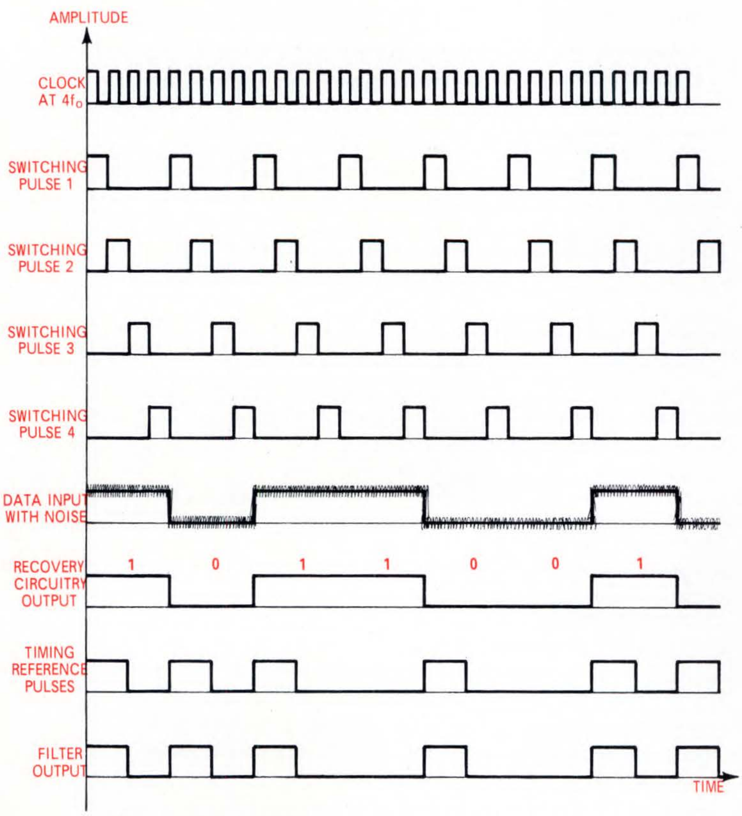

Fig. 2—**Waveforms** illustrate timing relationship of synchronous and in-phase signals (input and local clock) generated by the system in **Fig. 1**.

to "clean up" the pulses issuing relatively noise-free serial data for further processing. The recovery circuit consists of a lowpass filter for excluding out-of-band noise and a "1" or "0" decision-making device such as a crossover amplifier. Then a timing reference pulse generator produces a 50% duty cycle pulse at each transition (0 to 1 or 1 to 0) of the incoming data, because in a truly random **NRZ** (nonreturn to zero) bit stream there are no discrete frequency components present. Specifically, no component is at the bit rate.

Data transitions contain the frequency information. If a series of unidirectional pulses is generated to mark transition times, there will be a discrete component of the bit frequency f_0 in the generated pulse train.

The timing reference pulse train is applied to the commutating filter and switched through under control of the sequential pulses. Each time a pair of switches is closed, one-fourth of the input wave is entered into one of four RC networks. The voltage across the capacitors will equal the average value of one-fourth of the input wave. Since this occurs in all four RC networks, the filter output is similar to the input but somewhat truncated. When the input frequency differs from f_0, the accumulated capacitor charge or voltage will be less than that for the synchronous case. Therefore, the filter has a symmetric bandpass characteristic centered at f_0—the switching rate. The frequency where the filter response is 3 dB down is:

$$f_{3\,dB} = \frac{1}{2\pi N (RC)_s} \left[2^{\frac{1}{n}} - 1 \right]^{1/2}$$

where N = number of networks
n = number of RC sections/network
$(RC)_s$ = section time constant

To illustrate, assume N = 4, n = 3 and $(RC)_s = 7.92 \times 10^{-3}$ yielding $f_{3\,dB} = 2.56$ Hz, and a filter bandwidth of approximately 5 Hz.

A peak-to-peak detector converts the filter output signal to a dc voltage which is then compared with a reference voltage. When the output of the peak-to-peak detector is greater than the reference setting, the received signal is considered valid (below the threshold represents no signal). System bandwidth and the minimum S/N ratio at which the filter detects information are a function of this threshold setting. Both the peak-to-peak detector and threshold detector are IC operational amplifiers.

A COS/MOS 4-channel multiplexer (CD4016) is used to switch the digital input signal. The ON resistance for each channel is 425Ω. The 3-stage RC networks exhibit approximately 15 dB/octave rolloff, thus improving performance with wideband noise input.

System waveforms in **Fig. 2** represent data input

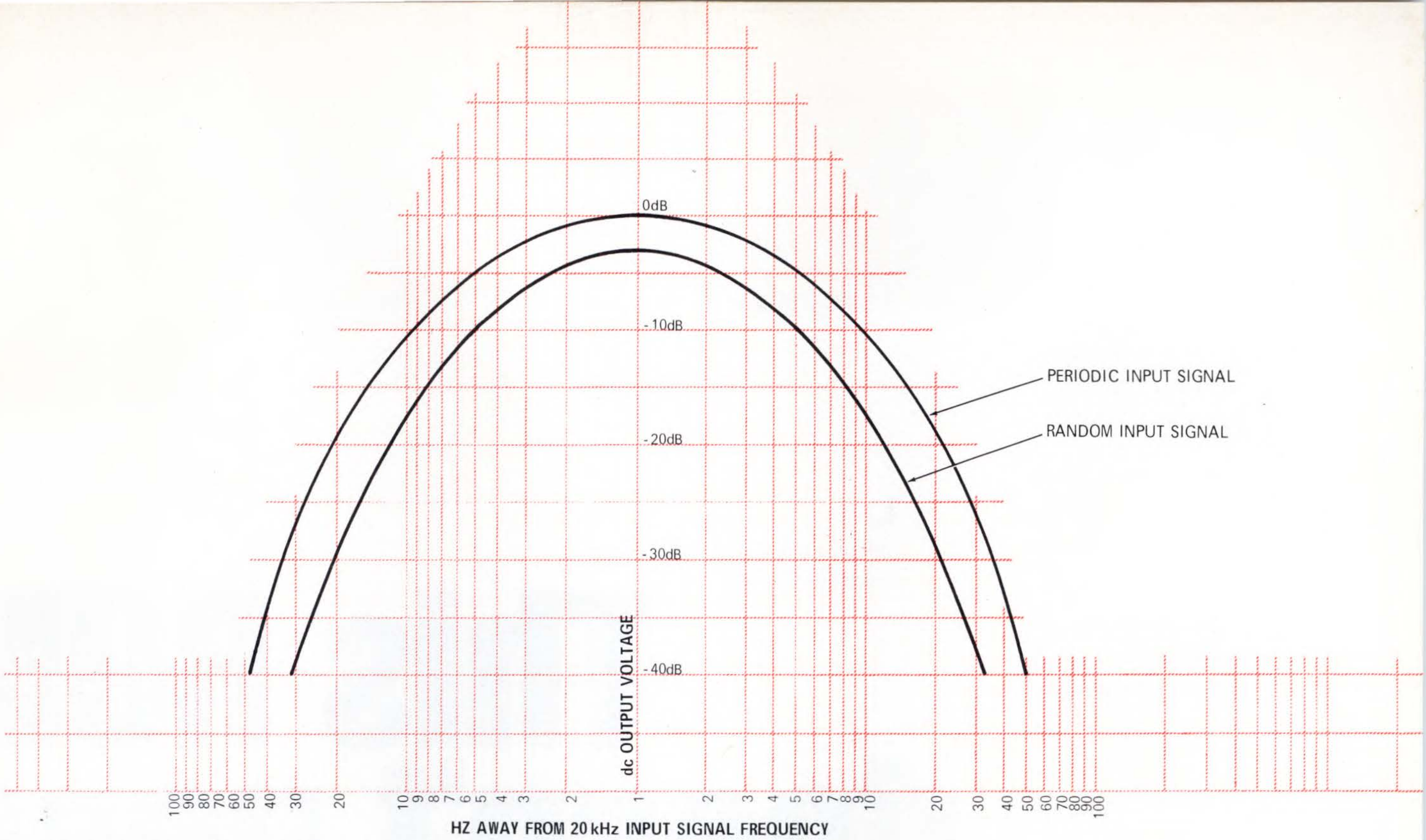

Fig. 3—**Measured output voltage** of the peak-to-peak detector vs input frequency for both random and periodic input signals.

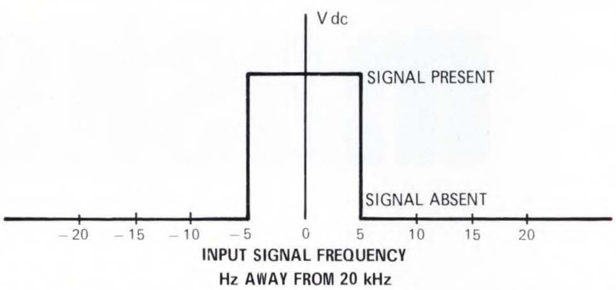

Fig. 4—**Output** of the threshold detector (**Fig. 1**) set for large S/N ratio operation.

and local clock signals which are synchronous and in-phase. For the asynchronous and out-of-phase cases, the average output voltage will be a truncated signal instead of an exact replica of the input signal.

System Characteristics. For the commutating filter in **Fig. 1**, the center frequency is 20 kHz with a measured 3-dB bandwidth of 7 Hz for a periodic input signal, 5 Hz for a random input. A resonant circuit with an equivalent bandwidth and center frequency has a Q-factor greater than 2500. However, the selectivity of the commutating filter is greater than the equivalent resonant circuit because the rolloff rate is greater. The measured filter peak-to-peak detector output voltage is plotted against input frequency for both random and periodic input signals in **Fig. 3**.

Threshold detector output, set for operation at large signal-to-noise ratios, is shown in **Fig. 4**. In this case the system bandwidth is 10 Hz, with a high output level occurring when the desired input signal is present, a low output indicating absence of a signal. For lower S/N ratio operation, the system bandwidth is increased. Reliable signal detection of a random binary input signal has been demonstrated at a −3 dB S/N ratio measured within the bandwidth of the input signal.

Typical response times for the commutating filter are 20 msec (attack) and 100 msec (dropout). Increasing the minimum S/N ratio at which information can be detected will reduce the dropout time.

The system logic is developed with COS/MOS devices. At relatively low clocking rates (< 1 MHz), COS/MOS circuits exhibit a substantial reduction in power dissipation compared to other types of digital circuits. In addition, these units offer high noise immunity and high fanout capability. Operating from a 9V dc supply, the filter and decision circuitry require less than 50 mW of power. This approach grants a considerable savings in both size and weight compared to the popular crystal filter. Also the commutating filter lends itself to microminiaturization through the use of hybrid techniques.

The effort described in this article was accomplished on the Bancroft program, Contract No. DAAB07-67-C-0263 from the United States Army Electronics Command, Fort Monmouth, N. J.

David A. Johnson is a senior engineer with the Electronics Div. of Avco Corp., Cincinnati, Ohio. His duties include designing and developing analog and digital electronic systems. Johnson attended the University of Kentucky, where he received B.S.E.E. and M.S. E.E. degrees.

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Millisecond/bit programing.

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Proven reliability.

This ROM doesn't need masks.

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Volume production, off-the-shelf delivery.

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Less than a penny per bit in volume.

Why wait around and pay more for one that does?

push, click click—BCD

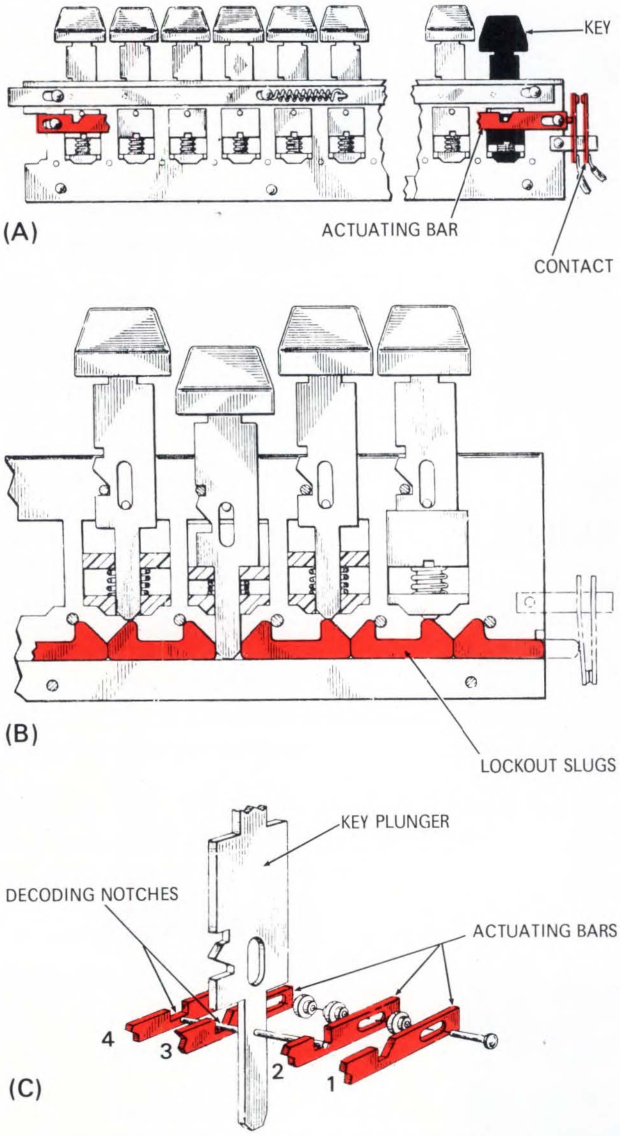


Fig. 1—**Side view (A)** shows the binary encoded switch (Pat. No. 3472973) and part locations. When the switch is pushed, the pair of contacts on the end will close if the notch is cammed.

View (**B**) illustrates the keyboard lockout capability. A selected key displaces the lockout slugs as shown, thus positioning the raised portion underneath the other keys. When the switch is released, the lockout slugs return to their normal positions.

Four actuating bars are required to perform BCD encoding for digits 1 to 15, as shown in (**C**). Each notch represents one bit (0 or 1) of any binary code. In this example, bars 1 and 3 would close their respective sets of contacts to generate a binary 5 (0101).

No electronic circuitry or power source is required for digital-to-BCD conversion in this unique keyboard. When a key is depressed, notched bit bars perform all of the necessary encoding.

Multiple-position and multiple-contact switches either of the rotary or ganged pushbutton type are the usual choice for most keyboard designs. A pattern of individual switch contact closures represents either the key's function or location—achieved by converting digital data into a binary code. Because of the number of contact closures normally required, the problems of wiring, solder connections and even the switch structure itself can place severe restrictions on the final design. The encoding switch to be described uses only a single contact to generate a binary bit at the output.

Obviously, a single contact conversion offers many advantages, mainly a reduction in solder connections and associated hardware such as wire. The concept is based on a set of notched bars or sliders (see **Fig. 1**). When a key is selected, the sliders respond and operate a pair of contacts. With multiple contact switches, the generation of 15 individual digits requires four switches and four actuating structures. Using the slider concept, however, only four actuating structures are needed. Thus substantial reductions in the number of switches, hardware and maintenance cost are realized.

How It Works. Several views of the switch structure are illustrated in **Fig. 1**. For converting digital information to binary, this structure operates a mechanical or actuating bar that closes a set of contacts located on the end of each bar. Each bar has a specific pattern of notches representing the desired output code.

There is a plurality of notch configurations (**Fig. 2**), each corresponding to a switch position. Whether the bar slides depends on the shape of the notch—square or cammed. If the notch is square, the bar will not slide when the switch is depressed. The camming surface will force the bar to slide and in turn, close the contacts. No motion defines a binary "0" and motion, a binary "1." Complete binary codes can be generated by logically combining the output contacts. The electrical interface for the encoding of 4-bit BCD is shown in **Fig. 3**.

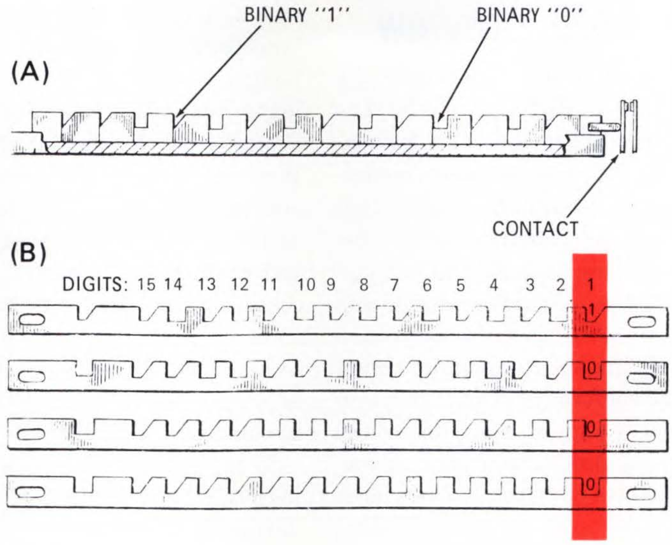


Fig. 2—**Cam surfaces** indicate binary "1s" and square notches "0s" in the actuating structure shown in (**A**). Diagram (**B**) illustrates the notch requirement for the BCD format of 15 keys.

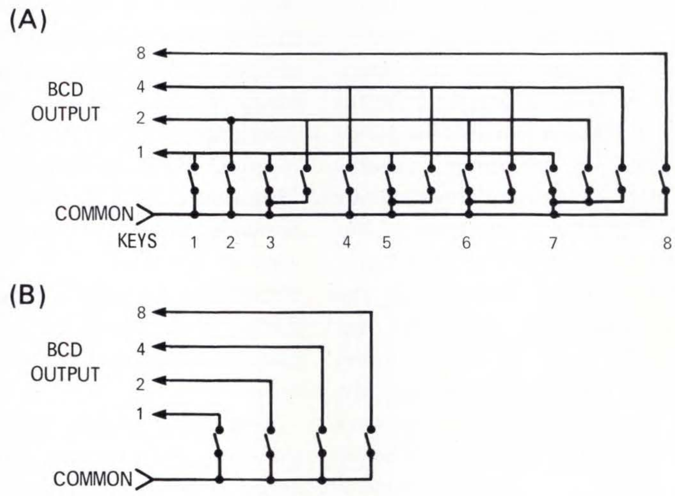


Fig. 3—**Encoding switch** not only simplifies the mechanical structure, but reduces the electrical interconnection. Diagram (**A**) illustrates the popular approach for generating a binary code through switch contacts as compared to (**B**) based on the encoding switch concept. Digit input positions 1 through 8 require various switching configurations and a number of contacts. For the encoded switch, four contacts provide a complete binary output for any number from 1 to 15.

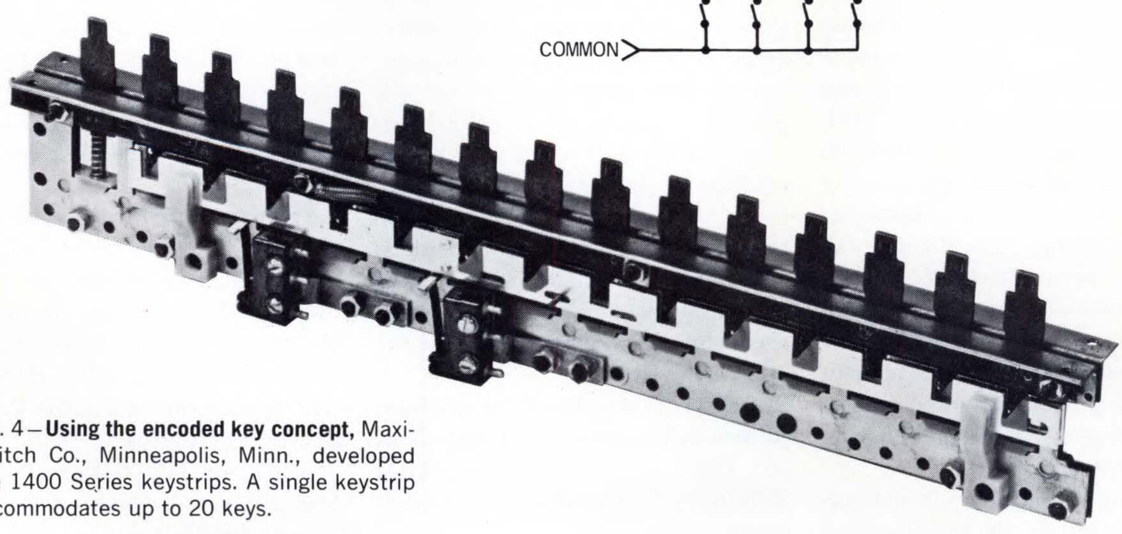


Fig. 4—**Using the encoded key concept,** Maxi-Switch Co., Minneapolis, Minn., developed the 1400 Series keystrips. A single keystrip accommodates up to 20 keys.

1971 FJCC preview

Approximately 200 exhibitors are expected to participate at the Las Vegas Convention Center on November 16-19. Ralph R. Wheeler, conference general chairman, projects that approximately 25,000 computer specialists, user representatives, managers, educators, officials and students will attend FJCC. In spite of less than favorable general economic conditions, the conference exhibit program shows every sign of being one of the largest and most diverse ever assembled. Displays of virtually every area of computer technology, including hardware, software and systems, will give the attendee a unique opportunity to evaluate and compare the latest offerings within the computer field.

"The jobs of engineers and scientists will be very different in the future. We will be responsible for greater degrees of planning, greater appreciation of consequences of our work and greater awareness of human values. Hopefully, we will lead." This theme will be examined by the keynote speaker, Dr. Arthur G. Anderson, IBM vice president. Commenting on the keynote session, Mr. Wheeler states that Dr. Anderson's recent studies and work at the Center for the Study of Democratic Institutions, combined with his managerial and research positions with IBM, provide him with unique credentials in assessing the broad potential of computer technology in improving the quality of life. In particular, Dr. Anderson's recent efforts at the Center have included traveling around the country to talk with university, government and industrial leaders in an effort to pursue ideas and proposals for bringing industry and academia closer together.

Dr. Frank Ryan, director of Information Systems for the U.S. House of Representatives, will deliver the luncheon address on Thursday, November 18, in the main ballroom of the International Hotel. Dr. Ryan, who as a quarterback led the Cleveland Browns to the National Football League Championship in 1964, is on leave from his position as Associate Professor of Mathematics at Case Western Reserve University. In his address, Dr. Ryan will describe the activities that are currently going on and that are anticipated in data processing for the House of Representatives. Special attention will be given to changes in traditions and to the adjustments the Representatives face in using new technologies.

In the technical sessions, approximately 67 papers will be presented during the three day conference. The papers cover a wide range of areas important to computer professionals and to others vitally concerned with the application of present and future computer technology. Included is coverage of such diverse sessions as "Computers in the Electoral Process," "Computer Assisted Instruction" and "Simulation of Computer Systems." Sessions involving computer hardware are:

SESSION 1—**Data Communications.** (Nov. 16, 10:30 a.m.) Chairman: F. D. LaRiviere, Control Data Corp.

Noncomplementary approaches to the same problem, i.e., cyclic redundancy checking in data communications systems. A panel discussion will provide critical analysis of the concepts presented. While it may be impossible to conclude which approach is the "best" or the most universal to the varying data communications environments, it might be possible to determine those areas in which one of the techniques is preferable over the other and why.

SESSION 2—**Applications of Computers in Emerging Nations.** (Nov. 16, 10:30 a.m.) Chairman: David Wilkinson, Hewlett-Packard International.

The rapid growth of EDP technology in the emerging nations is indicative of the importance placed on it by local governments. The uses to which this technology is placed and the manner in which state-of-the-art technology is transferred to the emerging nations are the subjects of this session. The questions to be covered include: How are computers now being used? How is the use of computers affecting the technical community? How should computers be used? What help is required in implementing computer technology in emerging nations?

SESSION 4—**Terminals** (Nov. 16, 1:30 p.m.) Chairman: M. T. Nigh, IBM Corp.

Cognizable advances in computer-supported terminals will be discussed. Experimental and original applications for terminals are emphasized covering experimental Picturephone, vocal data machine interface systems through plain paper printing and Braille terminals for the blind. The topics presented are in keeping with the advances being made in the computer application field throughout the technical and business world.

SESSION 6—**Images and Patterns** (Nov. 16, 1:30 p.m.) Chairman: Joseph Kuney, American Chemical Society.

Three topics will be presented within the area of graphic information processing. The first paper presents a new scheme for defining and generating images in parametric form. This approach involves a minicomputer controlling a photocomposing machine.

The second paper discusses the application of syntactic techniques to the problem of recognition of line drawings and patterns. The author illustrates his approach, using his own interactive system, called PARSE.

Of special interest is the third paper: an application of the computer and graphic information processing techniques to an area that has received little attention—music. The paper describes a system that recognizes and encodes printed music in machine language. The end result is the automatic rendering of printed music in a form suitable for machine processing.

SESSION 7—**Large Scale Integration** (Nov. 16, 3:30 p.m.) Chairman: Donald H. Weiss, IBM Corp.

Large scale integration into today's EDP equipment is mainly memories. They offer the distinct advantage of low cost and as the technologies develop, smaller and smaller sizes. The papers deal with approaches of systems implementation. Dynamic (FET) shift registers, ROMs and storage cells will be discussed. To some, LSI offers a panacea for logic development, to others, LSI is just another term in the technology vocabulary. The session will discuss some new aspects of LSI and will conclude with a panel discussion.

SESSION 9—**The User Interface for Interactive Search** (Nov. 16, 3:30 p.m.) Chairman: John L. Bennett, IBM Research Laboratory.

The theme for this panel discussion will be "what goes on in front of the terminal"—what facilities the user requires, what services the computer can provide and how the user responds to data display. Understanding the exchange of data between the user and the computer at the interface during search will enable the designers to build systems truly responsive to search needs.

Each panel member has researched the topic and will relate his own experiences. The discussion will highlight currently available findings that will help in the design of the link between the user—who understands the search results he wants—and the system designer—who can provide the means for achieving those results. Though the emerging interface technology is only roughly defined, we can begin to outline now the research and development issues to be resolved if interactive search is to achieve widespread user acceptance.

SESSION 10—**State of the Computer Art in Biology.** (Nov. 17, 8:30 a.m.) Chairman: Carol Newton, University of California, Los Angeles.

(Continued)

1971 FJCC *(Con't)*

Eminent biological investigators known for their creative use of computers in research will evaluate the present roles of computers in biological research ranging from molecular to population levels. Having proposed priorities for further development of computer hardware or software support in their fields, they will describe their current research efforts. The audience is encouraged to challenge these priorities and to suggest additional hardware or software development needed for biomedical research.

SESSION 16—**Computer Structures: Past, Present and Future** (Nov. 17, 1:30 p.m.) Chairmen: C. Gordon Bell and Allen Newell, Carnegie-Mellon University.

Since 1959, speeds of computer systems have steadily increased. These increases are the result of improved hardware, new computer structures and new computer applications. Still, one can observe that with the exception of the ILLIAC IV and the CDC STAR, most of the change appears to have resulted from the evolution of ideas that have been with us since the beginning of computing. Today, we can see that computer systems are still changing—witness the phenomenal growth of minicomputer installations. New memory and circuit technologies are on the horizon.

All of these considerations pose some challenging questions about the computing future:

—Are any of the new technologies revolutionary in their effect on computing?

—What will the computer structure be in 5 to 10 years?

—What additional technology developments will be required to get there?

—What science, at the computer structure level, is needed to get us there?

SESSION 17—**Computers In Sports** (Nov. 17, 3:30 p.m.) Chairman: J. Gerry Purdy, TRW Inc.

Sports and computers—an unusual interest forms the basis of a panel session. Experts in the field, including both developers and users, will discuss computer sports application areas such as football play analysis, ranking of football personnel for the college draft, auto racing timing, display systems, training modeling, etc. Analysis of these sytems will ask: Are they really useful? Other comments will be made to describe the future of sports systems and the application of the capabilities acquired through current systems to other fields. Panelists will also give their views on possible new application areas and answer questions about current systems.

SESSION 18—**Twenty Years in Passing** (Nov. 17, 3:30 p.m.) Chairman: Warner King, IBM Corp.

Twenty years have passed since the first "JCC," held in Philadelphia. From then until now the world has witnessed the phenomenal growth of the computer industry. We have almost reached the point of no return in our dependence on these machines. What were the participants of that first conference thinking about as far as future computer use was concerned? What were the problems they saw ahead in computer technologies? What surprises and disappointments have they experienced? This session is aimed at obtaining answers to these questions by having some of the original participants address these matters and others that may arise concerning the past 20 years.

SESSION 23—**Planning and Designing of High Performance Systems** (Nov. 18, 10:30 a.m.) Chairman: Charles Warlick, University of Texas.

The theme of this session is high performance requirements and systems. The first paper discusses strategies for selecting service alternatives. Three major alternatives are outlined, based on three different strategies: minimum risk, minimum change and integrated center. The second paper deals with real-time multiprogramming and the use of a new hardware monitor to provide time scheduling and real-time data interface. Linking of data processing systems via communication lines to achieve improved operational efficiency and lower costs for the integrated resource is the subject of the third paper.

Full conference fees for those who preregister, including both technical programs and exhibits, are $20 for AFIPS members and $50 for nonmembers. Registration at the time of the conference is $30 for members, $60 for nonmembers. Students and military personnel in uniform may register for $5. For further information on the conference, including registration and housing forms, write to: *1971 FJCC, c/o AFIPS, 210 Summit Ave., Montvale, N J 07645.*

coming soon...

FIRST NATIONAL CONFERENCE OF THE SOCIETY FOR COMPUTER MEDICINE, Nov. 18, Chicago, Ill. Society members plus guest will provide a cross section of association, academic, industrial and private practice interests in computer medicine. Preliminary activities for the one-day program include: keynote address, character member constitutional convention and assembly and special interest workshops. Cost for charter luncheon and conference manual is included in the registration fee of $20 for members, $30 for nonmembers. Preliminary program and advance registration forms are available from: *Society for Computer Medicine, 3839 26th St. N., Arlington, VA 22207.*

SOCIETY FOR INFORMATION DISPLAY (SID) 4TH ANNUAL CONFERENCE, Nov. 12, Dallas, Tex. Invited papers describe advances made in display hardware and software techniques, devices, systems and applications, including the following topics of interest: human factors, computer graphics, command and control, information systems and symbol generation. This conference is not restricted, but open to everyone interested in the display of information. The conference is sponsored by the Southwest Chapter, Society of Information Display (SID). For further information, contact: *D. R. Nance, Conference Chairman, Box 6015, M.S. 525, Dallas, TX 75222.*

coming courses...

COMPUTER-ASSISTED INSTRUCTION SYSTEMS, Nov. 1-12, Los Angeles, Calif. This course involves nearly 100 hours of computer laboratory and classroom instruction. About 40% of the time is spent on-line using a remote time-shared computer system. Each participant produces and debugs a lesson using CAI techniques. Programmed texts for 40 hours of premeeting activity, all course materials and on-line computer time are included in the $650 fee.

Knowledge of mathematics or computing theory is not required. Detailed course outlines and registration forms may be obtained from: *David P. Beyer, Professional Div., ETC, Box 49899, Los Angeles, CA 90049.*

10-WEEK COMPUTER INDOCTRINATION COURSE. This modularly constructed course, based on GTE Sylvania's experience is computer usage, covers all aspects of computer management and use of specific IBM equipment and programming via a variety of languages including BAL, PL/1, COBOL and FORTRAN. Other segments of the course deal with debugging techniques, use of decision tables and program documentation. The course is conducted on a periodic basis at the company's Data Processing Center or arrangements can be made for the course or segments of it to be presented at client locations. Additional details may be obtained from: *Joseph Rasmussen, GTE Sylvania Data Processing Center, 5700 W. Genesee St., Camillus, NY 13031.*

SEMINAR ON DATA COMMUNICATIONS SYSTEMS, Nov. 15-17, Washington, D.C. This introductory seminar is for the individual preparing for an on-line, real-time or other system that involves data communications. The presentation is designed as an overview to orient the potential user in system design aspects, hardware considerations and software organization and implementation. Further information is obtainable from: *Registrar, The Institute for Advanced Technology, Control Data Corp., 5272 River Rd., Washington, DC 20016. Telephone: 301-652-2268, Ext. 245.*

call for papers

IEEE REGION III CONFERENCE, April 10-12, 1972, Univ. of Tennessee, Knoxville, Tenn. Both tutorial and state-of-the-art papers that "scan the spectrum" of electrical engineering in theory and practice are solicited. Topics of interest include: Digital Signal Processing, Minicomputers, Electronics, Computer Applications, Systems Engineering, Computer Hardware and Communications. A 500-word summary and a 50-word abstract should be submitted in triplicate no later than Oct. 20, 1971. Papers should be planned for an oral presentation of 20 min. Authors will be notified of acceptance by Dec. 1, 1971, and the final paper should be submitted by Feb. 1, 1972. Technical Program Chairman is *Walter L. Green, Electrical Engineering Dept., Univ. of Tennessee, Knoxville, TN 37916.*

1972 INTERNATIONAL SYMPOSIUM ON FAULT TOLERANT COMPUTING, June 19-21, 1972, Boston, Mass. Topics of interest include Fault-Tolerant System Architecture and Design; Testing, Fault Location, Diagnosis and Recovery; Applications of Error Coding Techniques; Methods of Design Verification; Measures of Reliability and Related Parameters; Mathematical Modeling of Fault-Tolerant Computers; Error Control in Computer Networks; Graceful Degradation of Multiprocessor Systems; System Programs for Testing and Diagnosis; Operating Systems for Fault-Tolerant Computers; Hardware and Software Aspects of Software Reliability; Redundancy Methods in Logic Design; and Current Fault-Tolerant Computing Practice. Prospective authors must notify the Program Chairman before Nov. 1, 1971. Papers (2000 to 4000 words) are to be submitted for review by Dec. 1, 1971, with a statement (less than 500 words) explaining the nature of the contribution. Program Chairman is: *Prof. Gernot Metze, Coordinated Science Laboratory, Univ. of Illinois, Urbana, IL 61801.*

10TH INTERNATIONAL CONFERENCE ON MAGNETICS, April 10-13, 1972, Kyoto, Japan. Papers are solicited in all areas of applied magnetics, related magnetic phenomena and superconductivity. Digests must be received no later than November 20, 1971. A digest is a condensation of a paper into a two-page summary that contains an outline of the analysis or experimental work to be presented, including as much as possible the final results. Please quote numerical results whenever available. Figures and tables are encouraged. Digests should be sent to: *Professor Eiichi Goto, c/o INTERMAG 72 Secretariat, KDD Research & Development Lab, 1-23 Nakameguro 2-chome, Meguro-ku, Tokyo, Japan.*

another boost for credit cards—

Nortronics Company, Inc. will introduce their newly-developed DigiWand—a pencil-sized, azimuth-independent magnetic reader for use with point-of-sale digital systems—at the 1971 Fall Joint Computer Conference. DigiWand reads encoding formats presently established as standards by the American Bankers Association and the International Airline Transportation Association.

The key feature of the new magnetic reader is a circular gap configuration that sharply reduces digital error rate. Errors occur when the operator improperly passes the reader instrument over the magnetized stripe. With prior state-of-the-art techniques, the relationship between the linear head gap and magnetic stripe had to be close to or at 90°. However, DigiWand permits the operator to tilt the pen approximately 20° in any direction without sacrificing reading accuracy.

Typical specifications include 10-kHz read bandwidth, 250-bpi recording density, 15-ips wiping speed and inductance of 100 MHz. With a recording medium similar to 3M 777 tape, a read output of 2 MV pk-to-pk is obtained with a resolution of 85%.

Nortronics Company, Inc., 8101 Tenth Ave., Minneapolis, MN 55427.

420

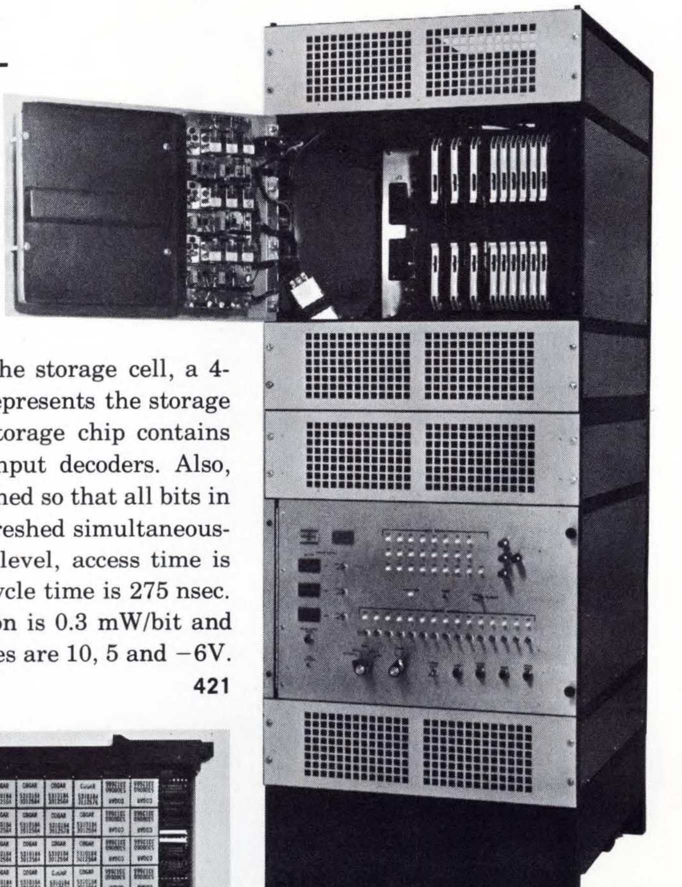
computer line features solid-state main memory—

Cogar's main memory system is the first MOS main storage for a computer—the ICL 1904S system. Organization of each main memory system module is 32,768 words by 25 bits or 96k bytes. System access time is <175 nsec worst case and cycle time is 275 nsec. Each ICL 1904S computer employs at least two modules.

The top unit in **Fig. 1** has the front test panel open to show the power control circuits located on the back side of the front panel, I/O cable sockets and the nine-card positions for three logic and six memory cards. The bottom unit portrays the system with the test panel in a closed position. Three logic cards provide self-test logic, interface logic and timing circuits as well as line drivers. The six memory cards offer a storage capacity of 32,768 words by 25 bits or 96k bytes. The power supplies and blower assemblies are behind the front grill panels. Two units, mounted on a trolley, roll into the ICL system cabinet.

The memory card (**Fig. 2**) has a 16,384 word by 9 bit configuration. Each storage module contains 2048 bits, organized as 2048 words by 1 bit—two n-channel MOS 1024-bit storage chips. The storage cell, a 4-device design, represents the storage cell and each storage chip contains the necessary input decoders. Also, the chip is designed so that all bits in the chip are refreshed simultaneously. At the card level, access time is <150 nsec and cycle time is 275 nsec. Power dissipation is 0.3 mW/bit and sequency voltages are 10, 5 and −6V.

421



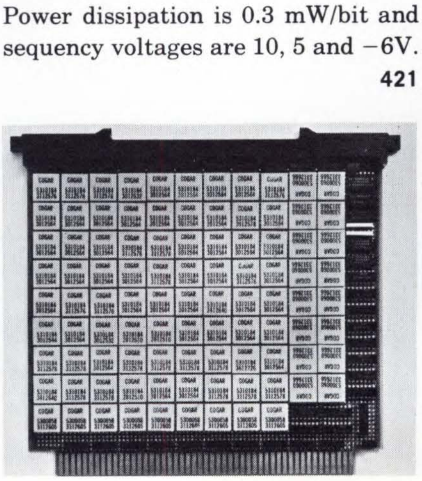


Fig. 1—**Two Cogar main memory system modules** (above) located one on top of another.

Fig. 2—**Basic memory card** has 16,384 word x 9 bit organization. **422**

MOS KEYBOARDS & DATAKEYS

MOS KEYBOARDS PROVIDE THE FOLLOWING OPTIONS:

- **ASCII Coding**
- **Custom Coding**
- **Multi-Key Roll-Over**
- **Interlock**
- **4 Mode Shifting**
- **Delayed Strobe**
- **Odd or Even Parity**
- **Repeat Function**
- **Output Latching**
- **TTL/DTL Compatibility**
- **Low Power Consumption**
- **Plug-in Code Changeability**
- **Wired-OR Capability**
- **Design Simplicity**

CUSTOM KEYBOARDS can be designed to your exact requirements using MOS or TTL logic circuitry.

DOUBLE SHOT LEGEND BUTTONS are available in a variety of sizes, colors and legends. Specials can be made to order.

RIGIDLY CONSTRUCTED ELEC-TROL KEYBOARDS employ a metal mounting panel to support the SNAP-LOCK DATAKEYS, thereby protecting the PC Board from operating stresses.

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Phone: (213) 788-7292
(805) 252-8330
TWX: 910-336-1556

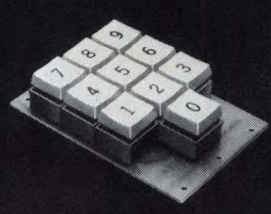
DATAKEYS ARE AVAILABLE INDIVIDUALLY allowing you to manufacture your own keyboards and arrays. These units employ a hermetically sealed contact providing a minimum of 20 million operations from low level to 10 watt loads.

SNAP-LOCK DATAKEYS are particularly suited for data terminal keyboards:

- Touch, feel and stroke
- Ease of Assembly
- No mounting hardware required
- Internal diodes available

LOW-PROFILE DATAKEYS are designed for calculators, portable equipment or wherever minimum height is required:

- .750" overall height
- Short Stroke
- Ease of Assembly
- Mounts directly on PC Board



KEY ARRAYS employing either **SNAP-LOCK** or **LOW-PROFILE DATAKEYS** are available. Custom arrays can be furnished to your exact requirements.

Reshaping concepts in electronic components and systems!

CIRCLE NO. 414

Progress in Products

New Armature Design Reduces Relay Response Time

PROGRESS IN MERCURY-WETTED RELAYS

Typical response time between 0.8 and 1 msec and reliable operation at 500 Hz are achieved in C. P. Clare's new HGQM Series of mercury-wetted relays.

Designed for switching low-level, sensor-based analog signals in process control, data logging/acquisition applications, the HGQM provides reliable operation with as little as 135 mW drive power at nominal coil voltage. The new relay is capable of switching 50 VA within its limits of 500V max and 1A max, and the transfer period is typically 100 msec.

A unique "T"-shaped hinged armature is both contact wetted and bearing lubricated by mercury (see **Fig. 1**) and replaces the conventional cantilever armature. According to C. P. Clare, this new armature is responsible for the significant improvements of the HGQM Series over other mercury-wetted relays.

Contact noise, as plotted in **Fig. 2**, is significantly reduced by elimination of spring type contact and the reduced mass of the new "T"-shaped armature.

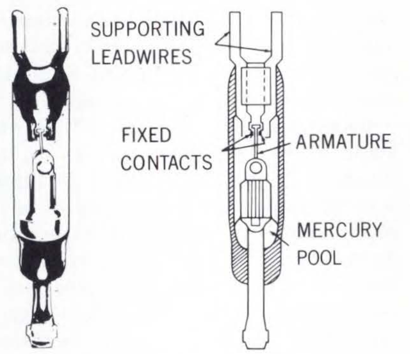


Fig. 1—Low-mass, "T"-shaped pivoted armature moving on a mercury lubricated bearing replaces the conventional stiff spring element in the new HGQM relay.

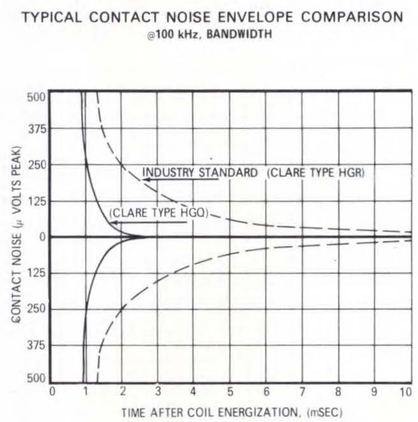


Fig. 2—Contact noise settling to 5 μV in 2 msec represents a significant improvement in electromechanical relays.

The form T relay, with random make-before-break or break-before-make action, is available in single and dual capsule modules and with single-side-stable or bistable adjustments. It also comes with single and double-wound coils, and with rated nominal coil voltages of 5, 6, 12 or 24V dc. Manufacturer-rated life is over 2 billion operations. Cost, in OEM quantities is $5 to $6/pole.

C. P. Clare & Co., 3101 Pratt Ave., Chicago, IL 60645. **149**

Double-Balanced Mixer Offers Low Price, High Performance

PROGRESS IN DOUBLE-BALANCED MIXERS

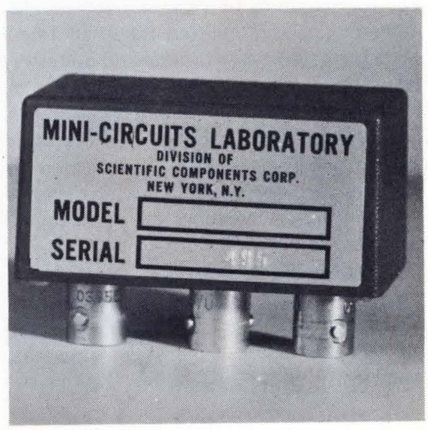
A price/performance breakthrough in connector-version double-balanced mixers is the result of high-volume production techniques brought on by an in-house development program at Mini-Circuits Laboratory.

Selling for $19.95 in quantities of 100, the Model ZAD-1 offers performance equivalent to units costing approximately twice the price. Well-matched, hot-carrier diodes are utilized to meet the unit's high performance standards that include: range of dc to 500 MHz, conversion loss of 5.5 dB throughout most of its frequency range (loss typically decreases to only 6.5 dB at 500 MHz) and isolation greater than 45 dB over the lower portion of its range falling to 30 dB, typically, at 500 MHz.

Standard connectors are either BNC or TNC with 3 mm SMA available for an additional $10. The units are double shielded and housed in a die-cast aluminum case with baked enamel finish.

Every production run is 100% tested to assure high reliability and the units carry a 1-year warranty.

Mini-Circuits Laboratory, Div. of Scientific Components Corp., 2913 Quentin Rd., Brooklyn, NY 11229. **150**



Automated Test Station Provides Maximum Flexibility

PROGRESS IN INSTRUMENTATION

The Fluke Terminal/10 automatic test terminal series offers many advantages besides automation of a test station. Most noteworthy perhaps is that the computer is not dedicated to the Terminal/10. The computer, as supplied by Fluke or by the customer, is left in standard configuration. Because all interfacing is done in the Terminal/10, the CPU is available for other tasks in addition to monitoring and controlling the test station. Other advantages include:

Expansion – Instruments can be added to the system at any time without influencing the CPU core size requirements.

Self check – All systems are supplied with self-check routines. These programs provide a rapid means of verifying system performance.

Manual programming – All instruments are manually programmable from either the interface programmer or the CRT terminal.

The Terminal/10 automatic test terminal is the direct result of Fluke's own need for automated testing. The need arose in 1969 when they introduced new products in the digital voltmeter and computer-interfaced instrumentation field. To be cost-competitive, production verification tests and final calibration had to be automated. Since January of this year, Fluke's DVMs and 4200 Series power sources have used the Terminal/10 for both subassembly and instrument level testing.

The system architecture consists of three main elements as detailed in **Fig. 1**. The first of these is a computer. Terminal/10 is compatible with most BASIC programmed computers. A typical computer used would be a DEC PDP-8 or PDP-11. With no wiring changes, the Terminal/10 can utilize non-BASIC engineering languages. With "16 USER BASIC" a PDP-11 can service up to 16 Terminal/10 test stations or any combination (up to 16, total) of Terminal/10 test stations and other terminals dedicated to other company needs. The second hardware element is analog instrumentation, usually built around Fluke instruments. The third element is the unit under test (UUT), and this can be anything from components to complete instruments.

To tie these three hardware elements together, two interfaces are required. These are the 1100A/10 interface processor for computer to system elements, shown in more detail in **Fig. 2**, and the 1200A/10 (rack mounted) or 1200B/10 (surface mounted) switch matrix units for the analog to UUT interface.

The 1200A/10 rack-mounted switch matrix is responsible for system self-check switching, accuracy enhancement and switching required to make nonprogrammable instruments programmable (instrument synthesis). The 1200A/10 also handles applications switching in the absence of the optional 1200B switch matrix.

The 1200B/10 is a surface mounted switch matrix for applications where several varieties of subassemblies and instruments are to be used. It is responsible for analog applications switching and also houses any custom UUT fixturing.

Both the 1200A and the 1200B will house up to 10 switch modules (called "blocks"). Each block contains 10 three-wire channels. Two of the three wires in each channel are "high" and "low"; the third is "guard." Any block may be converted to a 5-channel (4-wire plus guard channel) module for making Kelvin type connections. Alternately, any block may be replaced with a multibranch switch module. These general purpose, multibranch switch modules may be plugged, in any combination, into any 1200A or 1200B switch matrix mainframe. The primary application of a multibranch switch is to provide completely random analog connection between any combination (up to 10) of instruments and each of four terminals in a UUT. Thus, a mainframe containing 10 multibranch switch modules would allow random connection between 10 system instruments and 40 UUT terminals.

The multibranch switch module is organized into four branches of 10 channels each. Each branch is available to connect to a terminal of the UUT. Any combination of the 10 channels in a branch may be latched closed in a single programming step. Calls for combinations of contact closures in each branch may be programmed without closing any contacts, and a command to close all selected contacts within that switch module may then be issued to close all selected contacts simultaneously.

Each channel consists of a "low" terminal (not switched) which runs through the switch module from the system side of the switch matrix to the UUT side of the switch matrix, and a "high" terminal which runs from the system side of the switch matrix through the channel contact onto the "high" bus for that terminal on the UUT side of the switch matrix. Also, on the UUT side of the switch matrix, a UUT common terminal is provided to al-

(Continued)

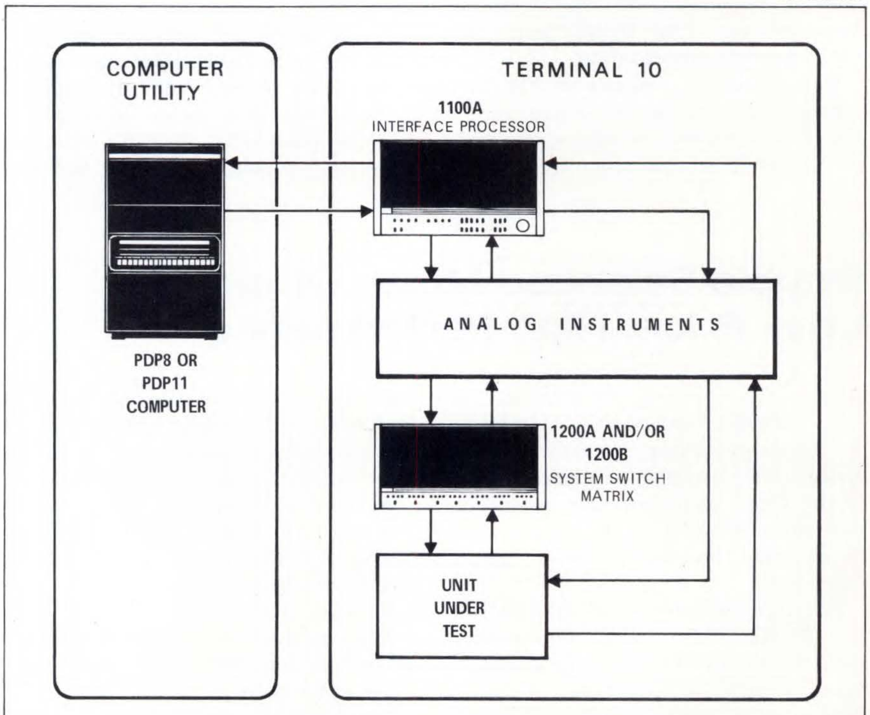


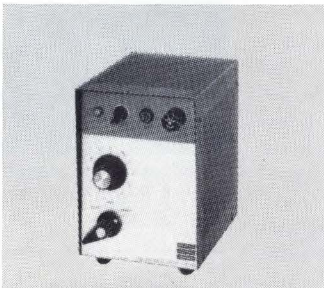
Fig. 1 – **System block diagram.**

(Continued)

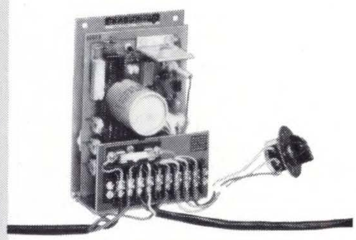
Bodine offers a complete line of fractional hp motors, gearmotors and speed controls

SPEED CONTROLS for Adjustable Speed Drive Systems:
A Bodine SCR-type speed control (chassis or encased) converts 50/60 Hz A-c to nearly pure D-c for shunt-wound drives. Makes possible smoother speed control of a Bodine drive (motor or gearmotor) over a wider range of speeds. For single source responsibility and maximum performance, insist on a perfectly matched Bodine motor—Bodine control system. A wide selection in the 1/50 to 1/4 Hp range is available.

The Bodine line, within its horsepower range, is unusually complete. There are over 3500 standard motors and gearmotors, with horsepower ranging from 1/2000 to 1/4. Bodine also builds custom and special motors to your design requirements. Our engineers will be happy to help you pinpoint the right one for your specific application need.

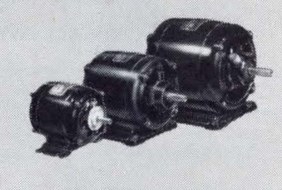


Encased Controls: Nine models are stocked. Some with extended speed range and/or torque control.



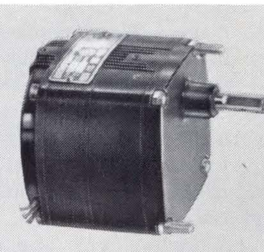
Chassis Control Kits: Four models stocked. Unlimited adaptability. Install in your own enclosure.

FHP MOTORS & GEARMOTORS:
Since 1905 Bodine has manufactured fractional horsepower motors and gearmotors. Close tolerance machining and careful attention to even the smallest detail of construction enables Bodine not only to produce better motors, but to produce them at a lower cost to customers in terms of value received. STOCK Bodine motors and gearmotors are available in all types and sizes within a range of 1/2000 to 1/4 Hp; torques from 0.3 Oz-in. to well over 200 Lb-in.



Type N Motors: Three basic sizes; 3.36″, 4.50″ and 5.68″ in diameter. Stock ratings from 1/125 to 1/4 Hp. Almost any type of winding.

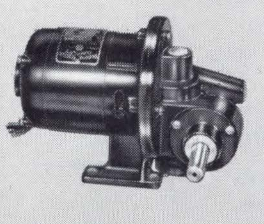
Type K Motors: Permanent-split capacitor instrument motors. Normal slip, high slip and synchronous windings. Stock ratings to 2.4 Oz-in. Only 2.405″ square.



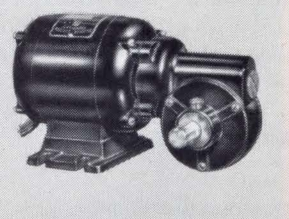
Type K Gearmotors: Permanent-split capacitor instrument gearmotors. Parallel shaft, helical gears. Stock ratings: 2.9-120 Oz-in. at 300-0.9 Rpm. Only 2.405″ square.

N-1D Gearmotors: Parallel shaft helical and spur gearing. Ratings to 25 Lb-in. Ratios to 900:1. Only 3.41″ square.

N-1R . . . single or double reduction worm gearmotors. Stock ratings to 5 Lb-in. range. Many ratios.



N-1RG . . . double reduction worm gearmotors. Stock ratings to 40 Lb-in. range. Many ratios.



Single reduction, right angle worm gearmotors. 5 frame sizes with stock ratings to 70 Lb-in range. Ratios to 60:1.

N-3RJ . . . double reduction right angle worm gearmotors for transmitting high torques at low speeds. Stock ratings over 200 Lb-in.

N-5RH . . . single reduction right angle worm gearmotors. Heavy duty reducer for continuous driving of heavy loads. Ample reserve for overloads. Stock ratings over 200 Lb-in.

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Test Station (Cont'd)

low electrostatic shielding of each channel from adjacent channels. Since no stimulus or measurement instrument currents flow through this shield, it resides at the same potential as the UUT common point.

Remote sensing may be accomplished by using two branches: one for "high" and one for "high sense" for each UUT terminal requiring such connections. The low terminal sensing is accomplished by hardwiring separate "low" and "low sense" lines out to the UUT common point.

Terminal/10 can be configured to virtually any function required. Capabilities and accuracies obtainable when configured as a precision-analog-instrument test-terminal (an example would be production line testing of precision multimeters) are tabulated in **Fig. 3**.

One of the most adaptable features of Terminal/10 is the operator's console, Model 1300A-01. This is an abbreviated 5-button keyboard. This keyboard (**Fig. 4**) simplifies technician-to-computer interfacing, bypassing the need for the full keyboard during most test and calibrate procedures.

In its simplest form—basically a data acquisition station consisting of a 100-channel scanner, a DVM and interface—Terminal/10 prices start at $15,000. More sophisticated systems range upward to $75,000 (plus a computer). From the basic configuration, the capabilities of Terminal /10 systems can be expanded and custom fitted to the customer's particular need.

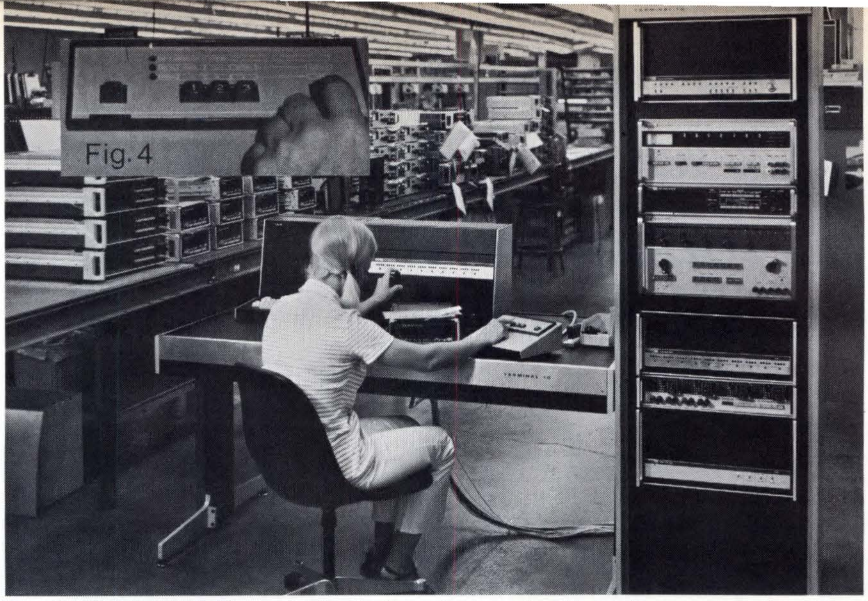
John Fluke Manufacturing Co., Inc., Box 7428, Seattle, WA 98133. **151**

Stimulus Capability	**Accuracy**
dc volts: 0-1 kV	±0.003%*
dc current: 0-100 mA	±0.006%
ac volts: 0-1 kV	
10 Hz-100 kHz	±0.02%
Ω: 1Ω-10 MΩ	±0.005%

Measurement Capability	**Accuracy**
dc volts: 0-1 kV	±0.005%*
ac volts: 0-1 kV	
10 Hz-100 kHz	±0.05%
Ω: 10Ω-10 MΩ	±0.01%
dc ratio	±0.005%
ac ratio	±0.05%

**Can be improved to ±0.001% by accuracy bootstrapping routine.*

Fig. 3—**Capabilities of the Terminal/10** when configured for verification and calibration as a precision analog test terminal.



Terminal/10 is available in 3 standard systems and with custom engineering, if required. Five—button console shown in **Fig. 4** (inset) handles most technician/computer interfacing.

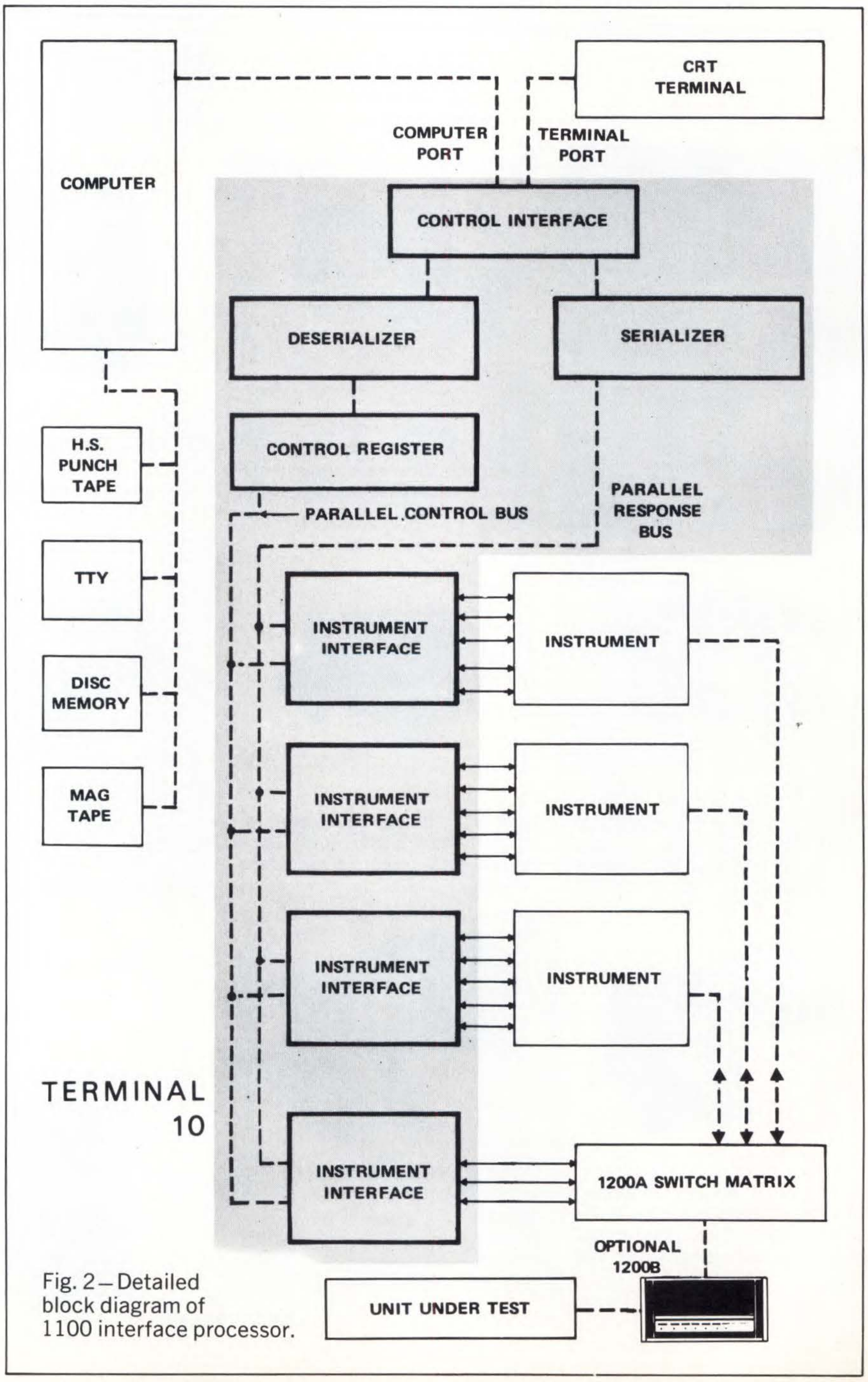
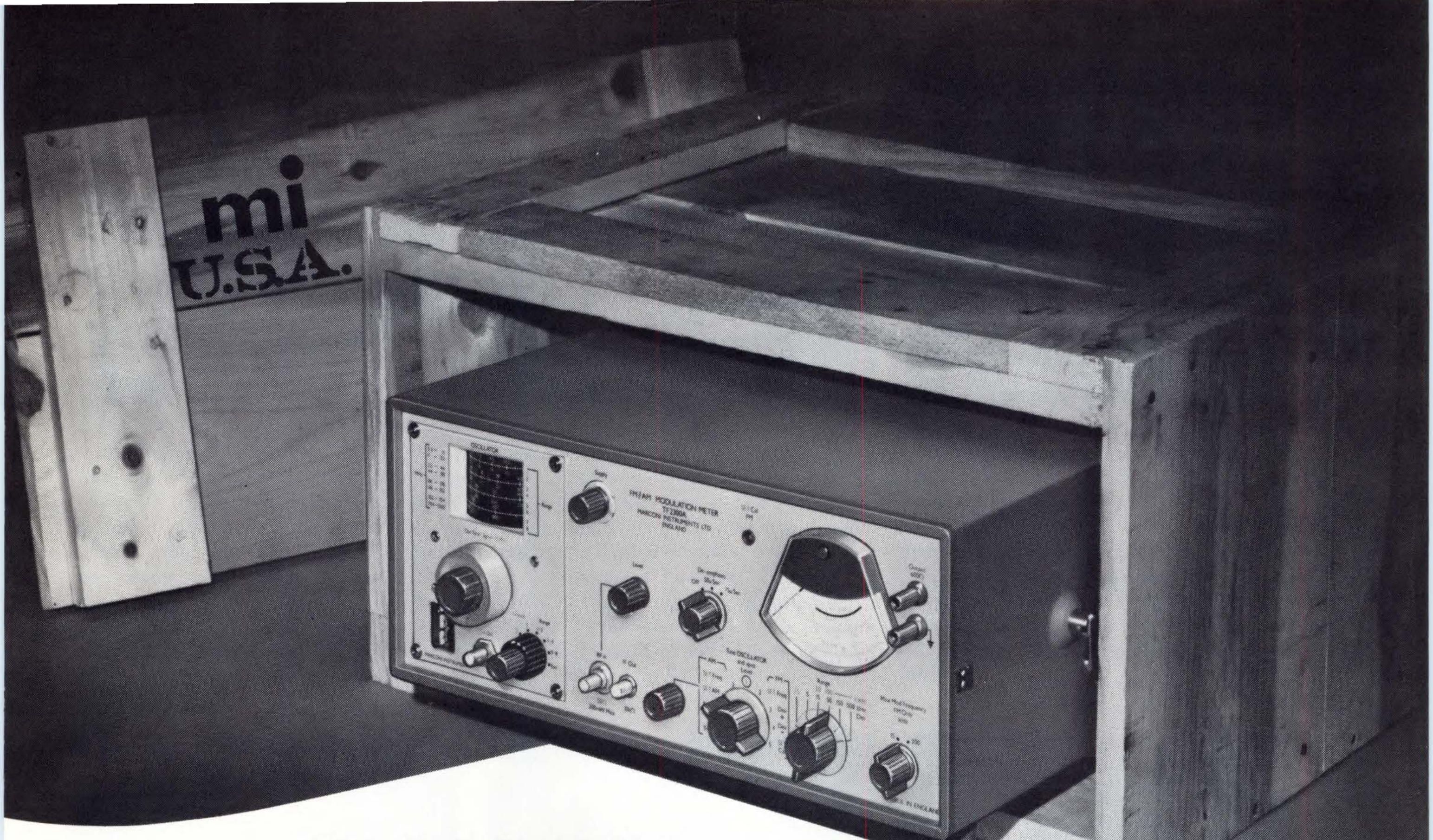
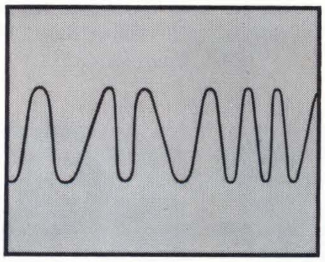


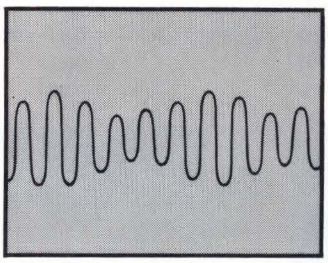
Fig. 2—Detailed block diagram of 1100 interface processor.



Model 2300A...
the Latest in this Unique Series of Solid State AM/FM Modulation Meters

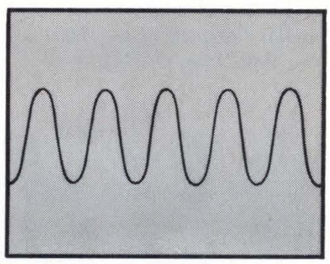


FM MEASUREMENTS
on carriers to 1 GHz (2.5 GHz with external oscillators). FM deviation, 6 ranges ± 1.5, 5, 15, 50, 150, and 500 KHz. Modulation frequencies 30 KHz to 200 KHz. Xtal controlled oscillator for low noise, low deviation measurements. Suitable for communications, particularly mobile, telemetry, FM stereo, etc.

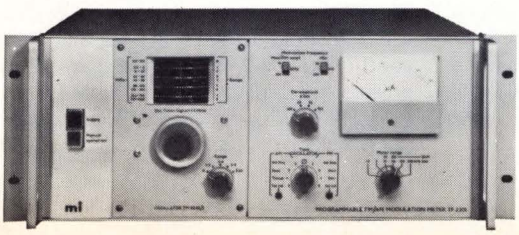


AM MEASUREMENTS
Two ranges of 30% and 100%. Peaks or troughs switch selected. Modulating frequencies 30 Hz to 15 KHz.

AM Rejection when making FM Measurements less than ± 1 KHz additional FM deviation error with 80% AM superimposed.



L.F. OUTPUT
Low distortion, low noise demodulated signal derived from FM or AM carrier. Switchable de-emphasis 50 μsec and 75 μsec. Level 0 dB into 600 Ω feeds distortion or wave analyser or external voltmeter for deviation measurements down to the order of 10 Hz.



Model 2301
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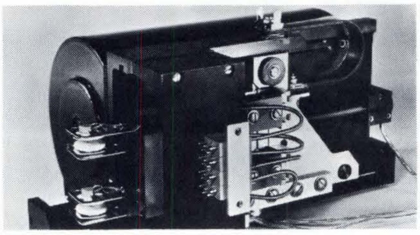
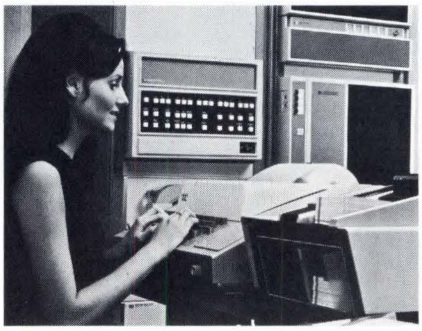
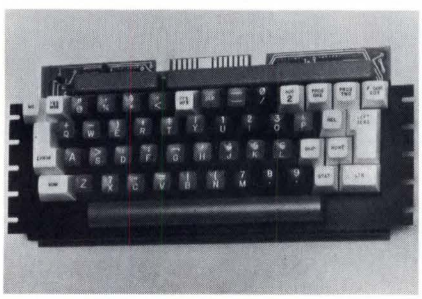


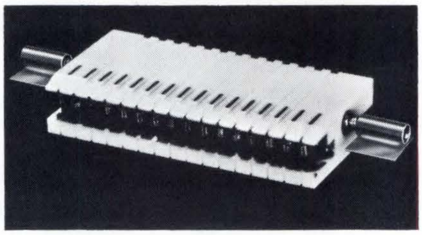
Head positioning system, Model 44, has been designed to position read/write heads on the IBM 5444, 2310 and similar cartridge disc drives. Track-to-track access time is 8 msec. One-third stroke (67 tracks is accessed in 50 msec, and full stroke (202 tracks) in 80 msec. Constant force stroke length is 2 inches, and total travel is 3.5 inches. Information Magnetics Corp., 5743 Thornwood Dr., Goleta, CA 93017. **160**



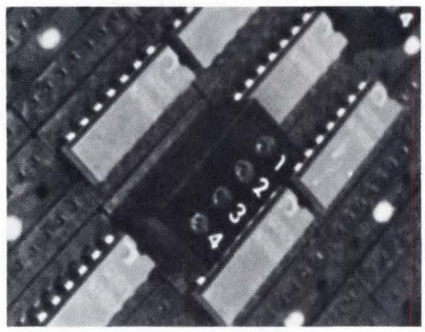
Disc-based small computer system, Model 2120A, combines the Model 2100A computer and Model 7900A moving-head disc with sophisticated software, including extended disc file management capability. Storage capacity is further increased with the addition of the Model 2883A disc drive. Hewlett-Packard Co., 1601 California Ave., Palo Alto, CA 94304. **161**



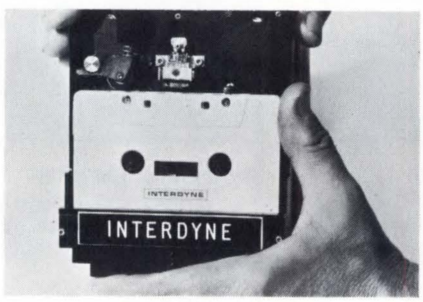
Keyboard, Model MK-29, offers L-shaped keys and deep-dished "home position" keys for added operational ease and efficiency. Standard features include 51 keys (MK-29/2011), encoded and function keys, two-key rollover, error and data lockout and DTL/TTL compatibility. The keyboards are insensivive to RFI and electrostatics. Typical power requirements are 5V, 180 mA. Data Electronics Corp., 12 Cambridge St., Burlington, MA 01803. **162**



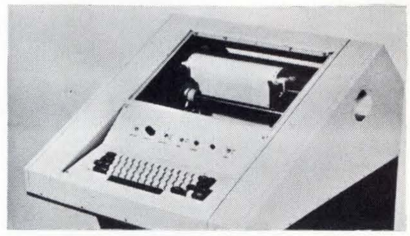
Sixteen-track flying magnetic head for head-per-track disc memories features a ceramic housing and flying height that can be adjusted to as low as 25 μinches to meet customer's performance requirements. Track width is 0.007 inch spaced on 0.06-inch centers. Inductance is 12 μH/winding leg and gap length is 110 μ-inches. External dimensions are 1 by 0.468 by 0.187 inch. Applied Magnetics Corp., 75 Robin Hill Rd., Goleta, CA 93017. **163**



Logic status indicator LL-4D provides four bits of logic status in a DIP. Light-emitting diodes give visible indications, low profile, long life and high reliability. Inputs are TTL/DTL compatible, and each input represents one unit load. In quantities of 1000, the price is $6.97 each. Unique Devices Co., Box 70, Bountiful, UT 84010. **164**

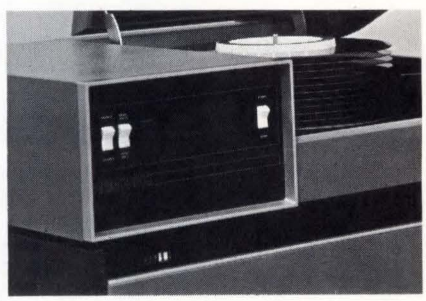


Cassette tape drive IC/2500 features a single servo-controlled capstan motor and a pair of individual reel motors for precise tape velocity and tension control. Recording rates are either up to 9600 bps synchronously or from one character at a time up to 30 cps incrementally. Available are a single-gap-head write/read unit for $995 and a dual-gap-head read-after-write configuration for $1200. Interdyne, 14761 Califa St., Van Nuys, CA 91401. **165**



Computer terminal, Model CD 3000, is a 10/15/30 cps system with full alphanumeric input/output, 132-character line, multicopy printout capabilities and an acoustic coupler. Full operation requires only a telephone and a 115V ac power outlet. Transmitted frequencies for mark and space are 1270 and 1070 Hz, respectively. Received frequencies are 2225 and 2025 Hz. Compudata Corp., Inc., 100 Manton Ave., Providence, RI 02909. **166**

Direct-access data set, Design 101, is a 300-baud system that operates with "Teletypes" as a functional equivalent of the Bell System 101C. Five versions are available. A built-in DAA function makes the unit adaptable to many applications. Prices range from $500 to $750. Design Elements, Inc., 1356 Norton Ave., Columbus, OH 43212. **167**



Disc drive 3665 uses a new recording technique to provide 480 million megabytes on-line. The bits/track are doubled and the rotational speed is reduced to 1200 rpm, thus maintaining 312 kbits transfer rate compatibility with the System/360. The 3665 consists of a 661 controller with a 665 (double density) adapter and from one to eight 665 drives plus spare. Unit accepts standard 2316 disc pack. Memorex Corp., San Tomas at Central Expressway, Santa Clara, CA 95052. **168**

Computer Products

Eight-channel optical mark sense card reader, Model 3260A, detects pencil marks or punched holes on hand fed cards. Each card has a maximum of 32 words and reading time/card is typically 1.5 sec. Unit price is $750. Hewlett-Packard Co., 1601 California Ave., Palo Alto, CA 94304. **169**

Shift register pack, Type SL-9, is a 1-bit, 5-zone circuit mounted in a ruggedized plug-in module. Frequency response of the device is 50 kHz max, and voltage requirement is ±20V dc. Square D Co., Dept. SA, Milwaukee, WI 53201. **170**

Disc surface test system ST-100 performs dynamic testing of 14 by 0.05 or 0.075 inch discs that are compatible with IBM disc packs. Simultaneous measurement of all parameters yields test times of 20 sec/surface. Three Sigma, Inc., 3 Computer Dr., Cherry Hill, N J 08034. **171**

A/D converters, 5000 Series, are high-speed units capable of 6-, 7- and 8-bit resolution at random or periodic word rates from dc through 10 MHz. The series consists of three models—5610, 5710 and 5810. Accuracy for this series is 0.2% ±1/2 LSB. Computer Labs, Inc., 1109 S. Chapman St., Greensboro, NC 27403. **172**

Dual-channel 128-bit programmable word generator, Model WG-116, provides both true and complement of either NRZ or RZ formats. Individual patterns are selectable from the front panel. Bite rate range is up to 15 MHz. Tau-Tron, Inc., 685 Lawrence St., Lowell, MA 01852. **173**

Digital cassette, Model 8123, combines use-proven high performance magnetic computer tape with a precision designed cassette case. The case—tough, high impact plastic and sonically sealed—is fitted with precisely-machined shims, guides, posts and pressure pads. In quantities of 12 to 47, unit price is $6.50 (quantity discounts are available). 3M Co., Magnetic Products Div., 3M Center, St. Paul, MN 55101. **174**

Electronic calculator, Model 8C, is a desk-size machine with an 8-digit readout, full four function keyboard, constant key, overflow and minus signs and both fixed and floating decimal point. Unit price is under $200. Eldorado Electrodata Corp., 601 Chalomar Rd., Concord, CA 94520. **175**

Computer Products

Modem DVM 1300 transmits significant quantities of data (1300 bps) as well as a quality voice channel on a single telephone channel. Unit operates in full-duplex mode over tie lines and half-duplex mode over dial-up network. Phonplex Corp., Subs. of Instrument Systems Corp., 410 Jericho Tpke., Jericho, NY 11753. **176**

Paper tape reader, Model AR10, reads all standard paper tapes in either direction at speeds to 75 cps and mounts in a 5- by 6- by 5-inch space. Unit employs photoelectric reading sensors with LEDs as the light source. Adtrol, Inc., 700 Abbott Dr., Broomall, PA 19008. **177**

Heavy duty perforator, Model P-1200, is a 120 cps unit that uses specially designed punch pins for extending the life of the mechanism. Prices are $1500 with quantity discounts available. Tally Corp., 8301 S. 180th St., Kent, WA 98031. **178**

Multiple channel recorder, Type 4211A, provides up to 50 hours of multiple channel capacity in one record pass. Both FM and direct versions are available from dc to 3 kHz. PCM units provide up to 8000 bps. Tele-Dynamics, Div. of AMBAC Industries, Inc., 525 Virginia Dr., Fort Washington, PA 19034. **179**

BOT/EOT sensor SS 403 for magnetic tape drives provides a "balanced" tape signal output, eliminating detection errors. Each of two channels in the assembly uses a LED and phototransistor pair. Spectronics, Inc., 541 Sterling Dr., Richardson, TX 75080. **180**

Synchronous tape reel drive maintains constant tension from 25g to 8 oz for uniform reels and longer tape life. For increased throughput, tape speeds up to 200 ips are available. FDC, 2560 W. Barberry Place, Denver, CO 80204. **181**

Automatic diagnostic system for data transmission network performs fast, accurate, end-to-end testing and can be operated by nontechnical personnel. Designated "Detect," the unit isolates faults in commonly used Bell-type data modems and in any terminal device or CPU having standard ETA interface. Data Products Corp., Telecommunications Div., 17 Amelia Pl., Stamford, CT 06904. **182**

Computer Products

Programmable timer/counter, Series 71, is basically a timer with each channel having a timing capability of 0 to 99.9 sec. A simple modification converts the unit to a counter of pulses rather than time. Struthers-Dunn, Inc., Systems Div., Bettendorf, IA 52722. **183**

Data generator SQ 320 performs functional testing of digital circuits, arrays and systems at repetition rates up to 25 MHz. A 12-bit parallel/32 word sequential format can be stored and presented on command. Frequency range is from 0.25 kHz to 25 MHz in six intervals. Adar Associates, Inc., 85 Bolton St., Cambridge, MA 02140. **184**

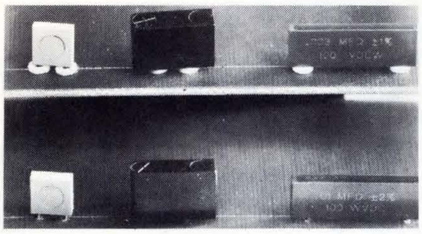
Tape perforator PER-820 operates at 20 cps asynchronously and mounts on a standard rack panel. Unit accepts logic input signals and comes complete with power supplies and tape handling. Data Specialties Inc., 1548 Old Skokie Rd., Highland Park, IL 60035. **185**

Add-on core memory for the PDP-15 computer, Model DMS-15, operates with an 800-nsec (max) cycle time and is available as either a 16 or 65k 18-bit memory. Unit recognizes an 18-bit address allowing indexed registration to 131k of core. Dimensional Systems, Inc., Subs. of Astrosystems, Inc., 393 Totten Rd., Waltham, MA 02154. **186**

Decoding unit converts standard telephone two-tone signal to 16 mA, 5V TTL outputs. A companion circuit delivers constant signal levels to the decoder. Both circuits require 5V supplies. Kenics Systems Corp., 125 Harvard St., Cambridge, MA 02139. **187**

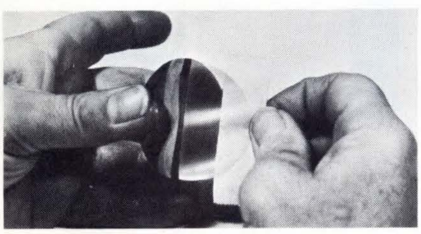
Cartridge tape system is plug-to-plug compatible with the NOVA family of minicomputers. Designated MiniDek, the system is complete with transport, controller, I/O cables and comprehensive system software. Complete system is priced at $2900 with OEM discounts available. Tennecomp Systems, Inc., 795 Oak Ridge Tpke., Oak Ridge, TN 37830. **188**

Digital current meter, Model 801AR, measures and displays peak magnitude of pulse currents (7 nsec wide) in the range of 0.01 to over 1A. Basic input sensitivity is mV/mA, input impedance is 1 kΩ and minimum bandwidth is 50 MHz. Scientific Measurement Systems, 351 New Albany Rd., Moorestown, N J 08057. **189**

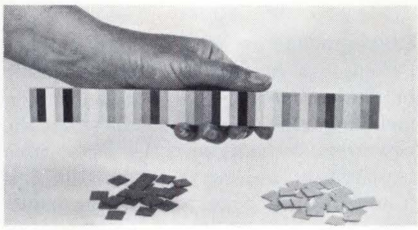


Wash away spacers, called Remov-A-Pads, are temporary devices for locating and spacing transistors, ICs and other components used in PC board assembly. Made from polymeric material, the spacers are noncorrosive, nonconductive and nontoxic. They dissolve easily in warm water as well as other organic solvents, and are not affected by soldering temperatures. They do not char, brown or distort and leave no residue. Dynaloy, Inc., 7 Great Meadow Lane, Hanover, N J 07936. **190**

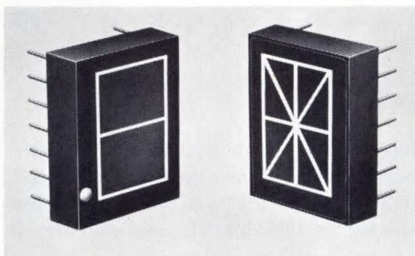
Electrically conductive coated windows, Type ECTC, are available with conductive coating with a nominal resistivity of 14.0Ω/square and 75% transmission of visible light. This coating may be applied to nearly all ceramic or plastic optical materials. Edges are terminated with pure silver resin buss bar borders for connection to mounting frame. Tecknit, 129 Dermody St., Cranford, N J 07016. **191**



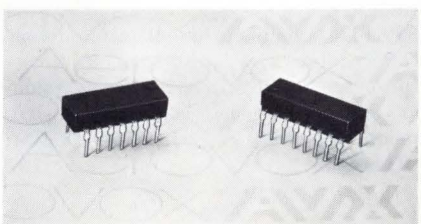
Protective spray coating, Silitect-2, may be used on either polished silicon wafers or glass photomasks to protect both from surface scratches. When applied and allowed to dry into a pliable film, about 30 sec, wafers or masks may then be stored with less attention to their protection. Removal of the film is made with a piece of transparent adhesive tape on one edge of the unit. The spray is available at $6/8-oz can or $60 for 12 cans. Controlyne Inc., Box 502, Allwood Station, Clifton, N J 07012. **192**



Step wedge accurately measures film thickness from 0 to 450 nm. With this scale, consisting of a calibrated color-step wedge (color vs thickness steps) and a quantity of precolored mirror plaques, visual color matching of initial and final colors on coated mirror plaques determine coating thickness to within 5 nm. Materials of any index of refraction, or degree of hardness (i.e., soft coatings and liquids) can be accommodated. Millis Research, Dover Rd., Millis, MA 02054. **193**

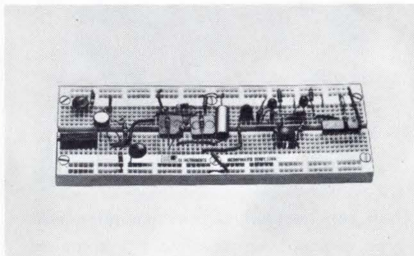


IC-compatible incandescent 5V readout modules provide 7000 fl brightness. The Dip 1050-Digital is a 7-segment device which mounts on a 0.300 inch, 14-pin dual in-line socket. The Dip 1050A-Alphanumeric is a 16-segment device which mounts on a standard 0.600 inch, 24-pin dual in-line socket. Pinlites Div., REFAC Technology Development Corp., 1275 Bloomfield Ave., Fairfield, N J 07006. **194**

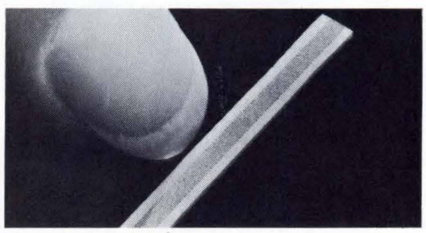


Monolithic capacitor arrays in 14- and 16-pin DIP packages employ multilayer chip capacitors and are available in prototype quantities with standard chip capacitors. For production quantities, the entire array can be fabricated as a single monolithic structure. Chip capacitors are provided in voltage ratings of 25, 50 and 100V dc and in capacitance ratings from 1 pF through 1 μF. Temperature characteristics available as standard are NPO, X7R and Z5U. Aerovox Corp., New Bedford, MA 02741. **195**

Miniature preset thermostats, "Tiny-Stats," are snap-acting thermal switches available for off-shelf delivery. The smallest snap-acting hermetically sealed thermal switch produced, they are available preset to operate in a temperature range from 150 to 275°F and are rated to switch up to 1.0A for 10,000 cycles. Devices outside this temperature range can be furnished/customer requirement. Texas Instruments Incorporated, 34 Forest St., Attleboro, MA 02703. **196**



Universal component sockets, Type El, allow interconnection with solid wire from 22 to 26 gauge. Each terminal has five tie points, one for component lead, three for input/output wires and one for test probe. Contacts are spring loaded beryllium copper, heat treated and nickel plated. Cost is $18. El Instruments Inc., 61 First St., Derby, CT 06418. **197**



"Photobar" is a new line of cadmium sulfide and cadmium sulfo-selenide photodetectors. Three basic materials are offered with peak spectral responses at 515, 575 and 625 nm. On resistance, with respect to material, is 200, 500 and 1000Ω when measured at 10 fc. "Dark" resistance values are typically above 1 MΩ. Standard length is 1 inch; other lengths are available on request. Price is $9.20 each in 500 quantities. Allen-Bradley Co., 1201 S. Second St., Milwaukee, WI 53204. **198**

Components/Materials

Sheet graphite for EDM electrodes, called Poco, is isotropic and flows current equally in all directions. Available in five grades, including copper-impregnated types, the new graphite material is flexible at room temperature and can be obtained in rods from 1/16-inch diam, sheets from 0.005-inch thickness and blocks up to 2 by 4 by 18 inches. Electrotools, Inc., Box 33, Broadview, IL 60153. **199**

Thin-film chip resistors are available with resistance values from 0.5 to 10Ω. Three sizes provide power dissipation of 50, 75 and 100 mW. Standard temperature coefficient is ±100 PPM/°C from −55 to 150°C; ±50 and ±25 PPM are available on special order. Prices range from $0.37 to $1.45 per chip. Film Microelectronics, Inc., 17 A St., Burlington, MA 01803. **200**

Incremental shaft encoders, TRU-ROta Series designed specifically for English-metric measuring systems, may be considered as two dual-channel encoders in one package. One system provides 100 and 254 pulses/revolution, the other 500 and 1270. Electrically the units operate up to 15V dc from a single power supply at frequencies up to 50 kHz. Prices start at $256.90. Trump-Ross Industrial Controls, Inc., 265 Boston Rd., North Billerica, MA 01862. **201**

Modular terminals are snapped into steel rails to provide a space saving of at least 33%. This complete line of terminals accommodates wire sizes from 27 gauge through 4/0 with wire wrap, screw, solder or clip connections. Hathaway Instruments, Inc., 5250 E. Evans Ave., Denver, CO 80222. **202**

PC board plug/receptacles are available in 17, 19, 23, 29, 35, 47, 49 and 51 contact sizes. The 42 Series plug assembly requires no secondary staking, and the single leg per contact eliminates 50% of the PC board hole requirements. Mating receptacles, Series 40, are available with or without card guides. Prices are $1.99 to $4.91 for 19-contact version. Methode Electronics, Inc., 7447 W. Wilson Ave., Chicago, IL 60656. **203**

Components/Materials

Fast curing structural adhesive chemically cures at room temperature. Type 3532, a new easy-to-use, two-component structural adhesive that starts curing at room temperature in 7 to 10 min, provides flexible high strength bonds on metals, plastics and wood. The adhesive develops 25% of its strength in 3 hrs and 100% in 24 hrs. Mild heat will accelerate the cure. 3M Co., 3M Center, St. Paul, MN 55101. **204**

FEP Teflon film with silicone adhesive offers excellent dielectric characteristics and can withstand up to 8500V ac. Series 2355 pressure-sensitive electrical tape comes in standard 18- or 36-yd rolls, has a total tape thickness of 3 mils, breaking strength of 6 lbs/inch width and a temperature range of −100 to 400°F. Dodge Industries, Inc., Hoosick Falls, NY 12090. **205**

Dielectric and thick-film glass coatings for screen printing are available. Materials in this new series are colored with permanent dyes and can be used for optoelectronic devices. ESL 4770B (black opaque), 4770BC and 4771BC (translucent blue) low-temperature dielectrics and overglazes can be used on soda lime glass substrates. 4608 (black) and 4608C (black) are compatible with gold cermets and may be used on alumina ceramics. Electro-Science Laboratories, Inc., 1133 Arch St., Philadelphia, PA 19107. **206**

Miniature tantalum capacitors have an average cost of $0.10 each in production quantities. The DIT Series is made from high grade tantalum pellets with epoxy coatings. Values range from 0.1 to 100 μF with ratings from 3 to 35V dc. Capacitor Div., International Electronics Corp., Melville, NY 11746. **207**

Bus bars for high-current capacity have either copper or aluminum conductors with a fused and bonded epoxy insulation. Connecting tabs are placed at each end for end-to-end connection. Threaded connecting studs are provided for wire connection, and a series of reach-through uninsulated pads allows mechanical or solder connections. Methode Manufacturing Corp., 1700 Hicks Rd., Rolling Meadows, IL 60008. **208**

Components/Materials

High-temperature heaters utilize all inorganic, inert materials to create a semi-flexible heater capable of operating in the 1000°F range. A new process allows the heaters to be manufactured in thicknesses <0.02 inch. Thermo-O-Lab Corp., 6940 Farmdale Ave., North Hollywood, CA 91605. **209**

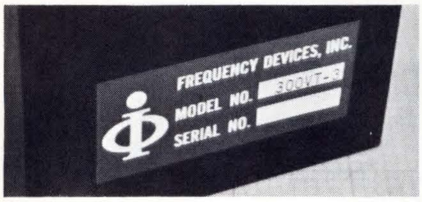
Alkaline immersion cleaner for printed circuit boards, called Enplate PC-453, prepares both single and multi-layer printed circuit boards for electroless plating and uniform thru-hole plating. For more complex cleaning operations it can be used electrolytically. It is supplied as a liquid concentrate which is diluted with water and operated at 170 to 200°F. Enthone, Inc., Box 1900, New Haven, CT 06508. **210**

Compact time-delay relay, Type 613, is a delay-on-operate relay with either 5 or 10A DPDT contact output. Ranges are 1 to 100 sec as specified on fixed delays. External resistor-adjustable delays over the same range are feasible. Midtex, Inc., 10 State St., Mankato, MN 56001. **211**

Photovoltaic infrared detectors for operation in the 8-12 micron region, IR101 A and B, feature high detectivity and response time of less than 15 nsec. The units are lead tin telluride and are comparable to copper or mercury doped germanium in detectivity but do not require cooling to low temperature. The basic model is priced at $1995. Raytheon Co., Foundry Ave., Waltham, MA 02154. **212**

Time delay module, Series 300, is a solid-state unit with an operate time delay of up to 5 min determined by external resistors. The module is designed to mount with a class E relay in an EIN socket, but it may also be used with a separately mounted relay or rotary stepping switch. GTE Automatic Electric, Inc., Northlake, IL 60164. **213**

Lithium formate harmonic generation crystals are suitable for efficient second harmonic generation of laser radiation. The second harmonic efficiency of lithium formate has been found to be approximately twice that of lithium iodate and 20 times that of KDP for 1.06 nm fundamental power. Crystals are available in apertures up to 2 by 2 cm and lengths up to 4 cm. Isomet Corp., 103 Bauer Dr., Oakland, N J 07436. **214**

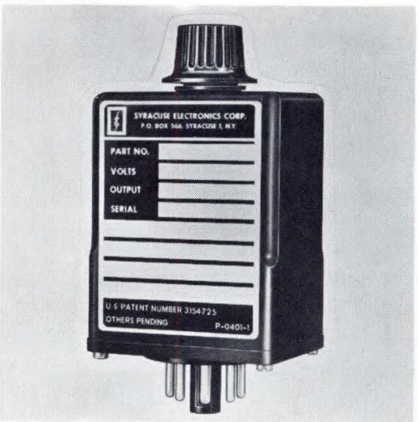


Voltage tunable active filters, Series 300, are 2-pole devices with cutoff frequencies that vary linearly over 20:1 range by application of a 0.5 to 10V control signal. Five models cover the 0.1 to 20 kHz frequency range. Specifications include ±0.2 dB passband gain, ±2% cutoff frequency, 1% linearity and 0.02 dB distortion. Custom modifications are available. Frequency Devices, Inc., 25 Locust St., Haverhill, MA 01830. **215**

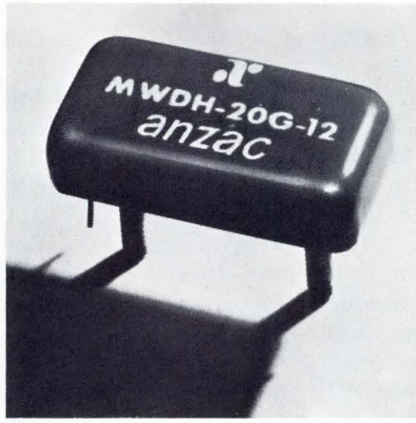
D/A converter, Model 310-12, is a 12-bit device developed for the graphic market. The unit includes the multiplication function and features <5 μsec settling time full scale. Full-scale output is 2 mA with up to 1.25V available. Linearity is ±0.05% max, full scale and drift with temperature is approximately 15 PPM/°C. The unit sells for $145 (1-9). Hybrid Systems Corp., 95 Terrace Hall Ave., Burlington, MA 01803. **218**

Modular power supplies, Models ZM15100-K and ZP51000K, feature 220V ac (60 to 400 Hz) operation with no derating from −25 to 71°C. Model ZM15100K supplies a dual, regulated output of ±15V at 100 mA and ZP51000K a single output of 5V at 1A. The same supplies are available for 12V ac operation. Prices (1-9) are $49 (ZM15100K) and $73 (ZP51000K). Zeltex Inc., 1000 Chalomar Rd., Concord, CA 94520. **221**

Instrumentation amplifiers, Models 4251 and 4252, are gain programmable over the 1 to 1000 range using one resistor. Other specifications include 2 μV/°C input offset voltage drift, <1 nA/°C bias current drift and 30 MΩ common-mode input impedance. Price in 100 quantities is $62 each. Teledyne Philbrick, Allied Drive at Rte. 128, Dedham, MA 02026. **216**

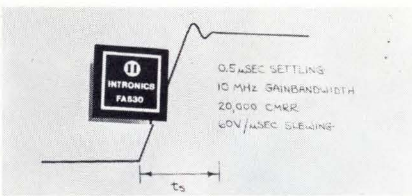


Solid-state time delays, TSR and TSS, are of the fixed and adjustable type for industrial and commercial applications. The TSR has a dpdt, 10A output and the TSS has an spst, 2A output. Both are available for 12 to 230V inputs and time ranges from 0.1 to 480 sec. Syracuse Electronics Corp., Box 566, Syracuse, NY 13201. **219**

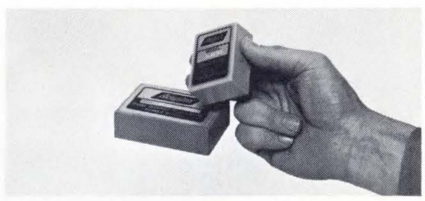


Amplifier, Model MWDH-20G-12, features 20 dB gain (at 10 MHz) and low intermodulation distortion in a plug-in package. Unit operates from 500 kHz to 100 MHz with a frequency response that is flat to 0.5 dB. Typical noise figure is 4.5 dB at 30 MHz, 5 dB at 60 MHz. Anzac Electronics, Div. of Adams-Russell Co., Inc., 39 Green St., Waltham, MA 02154. **222**

Eight-bit D/A converter, Model MN 316H, has guaranteed specifications for the full military temperature range. The unit provides a bipolar output of 5 to −4.961V with 1/2-bit linearity. Slewing rate is 0.5V/μsec, and settling times are 3 μsec for typical voltage output changes and <1 μsec for incremental changes. Prices range from $79 (1-4) to $67 (25-99) each. Micro Networks Corp., 5 Barbara Lane, Worcester, MA 01604. **217**



Differential FET op amp FA530 features 0.5 μsec settling time to 0.01% in either inverting or noninverting modes. Other parameters include 10 MHz gain-bandwidth product, 60V/μsec slewing rate, 20,000 CMRR, 50,000 open-loop gain, 50-pA input bias current and 20-mA output current. The unit sells for $36 in single quantity and comes in a 1.125- by 1.125- by 0.4-inch case. Intronics, 57 Chapel St., Newton, MA 02158. **220**



Power supplies of the E Series now include models with up to 50V and up to 500 mA outputs. More than 400 single and dual output models make up this series, all with trimming adjustments. Regulation for most models is ±0.05%, ripple 0.5 mV rms. Standard input is 105 to 125V ac, with provision for 210 to 250V ac inputs available as an option. Prices range from $30 to $78 each. Acopian Corp., Easton, PA 18042. **223**

Power amplifier (100W) covers the frequency band of 405 to 450 MHz. This amplifier features power output control over a 23-dB range, flatness of ±0.2 dB over the frequency range and an input VSWR of 1.5:1. Microwave Power Devices, Inc., 556 Peninsula Blvd., Hempstead, NY 11550. **224**

Solid-state chopper NS8000A comes in a TO-5 enclosure. The unit has transformer isolation and operates from dc to 1.5 MHz. Applications include low-level and high-speed modulation, demodulation, commutation and switching. Solid State Electronics Corp., 15321 Rayen St., Sepulveda, CA 91343. **225**

Reflective and absorptive variable attenuators, 504N and 554N Series, find use in applications requiring attenuation ranges of 100 dB. These units come in octave bandwidths from 0.5 to 18 GHz. Hyletronics Corp., Newtown Rd., Littleton, MA 01460. **226**

Double-octave hybrid coupler, Model ED-80, features amplitude balances of ±0.4 dB from 2 to 4 GHz and ±0.5 dB from 4 to 8 GHz. Power handling peak is 8 kW with an average of 200W. Unit meets MIL-E-5400 and MIL-T-5422 Class II specifications. Microwave Products Group, Sanders Associates, Inc., Grenier Field, Manchester, N H 03103. **227**

DC-to-dc converter, Model 2033, provides ±5 or ±2.5V dc output at 100 mA max with 28V dc input. Combined regulation is better than 10 mV for line and load changes with typical TC of 0.01%/°C. Prices are $85 (single quantity) to $79.50 (25-49). B. H. Industries, 5794 Venice Blvd., Los Angeles, CA 90019. **228**

High-voltage silicon bridge rectifiers have peak-inverse-voltage ratings of 1000 to 6000V at 50 mA. True rms voltage is 700 to 4200V. Dimensions are 0.75 by 0.75 by 0.25 inch, and the terminals are solder lugs. Computer Diode Corp., Pollitt Drive S., Fair Lawn, N J 07410. **229**

Optical isolator FPLA 810 has coupling efficiency of 10%, typical isolation resistance of $10^{11}\Omega$ and minimum voltage isolation between input and output of 750V. Prices are $2.55 (1-99), $1.70 (100-999) and $1.55 (1000+). Fairchild Camera and Instrument Corp., Microwave and Optoelectronics Div., 3500 Deer Creek Rd., Palo Alto, CA 94340. **230**

High-voltage CRT supply, Series 700, is designed for display system application. Available output voltages are 10, 12, 15, 18 and 20 at low max. Price ranges are $100 to $120 (1-9) and $70 to $82 (500). Walden Electronics, 223 Crescent St., Waltham, MA 02154. **231**

Up/down counter and decoder, Model U-4000, is a panel-mounted module, with fluorescent readouts that are visible for over 40 ft. Behind-panel depth is 1.2 inches, and there is one mating connector. Price in quantities of 25 is $126 each. Display General Inc., 241 Crescent St., Waltham, MA 02154. **232**

Frequency-to-dc converter, Series ST2000, features 1-5 mA, 4-20 mA, 10-50 mA or 1-5V dc outputs, 0.2% accuracy and adjustable alarms. Unit accepts inputs as low as 0 to 10 pulses/sec. Price is $135 each (OEM). Dynalco Corp., 4107 N.E. 6th Ave., Ft. Lauderdale, FL 33308. **233**

Broadband, low-pass EMI filter series, 2- and 3-wire types, offers a selection in the 120/208 and 250/440V ac standard ratings. Available configurations include "PI", "L" and "Double L" for 10 to 50A applications. Prices start at $10 each. The Potter Co., Div. of Pemcor, Inc., 500 W. Florence Ave., Inglewood, CA 90301. **234**

Picket generator, Model 6050, provides pickets having −33 dBm minimum output power levels spaced 25 MHz apart over the 250 to 1000 MHz frequency range. The unit comes in a 4.5- by 1.6- by 1-inch all-metal housing weighing 6.5 oz. Zeta Laboratories, Inc., 616 National Ave., Mountain View, CA 94040. **235**

Hybrid amplifier CA601 exceeds −66 dB intermodulation distortion. Typical gain of 30 dB covers the frequency range of 40 to 300 MHz with ±0.5 dB response flatness. In 100 quantities, the price is $65 each. TRW Semiconductor Div., 14520 Aviation Blvd., Lawndale, CA 90260. **236**

Twelve-bit D/A converter DAC-12QZ is a pin-for-pin replacement of its predecessor, Model DAC-12QS, and lists for $49 in 100 lots. Key characteristics include ±1/2 LSB linearity and 30 PPM/°C temperature coefficient. Output settles to 0.0125% in 5 μsec. Analog Devices, Inc., Rte. 1 Industrial Park, Box 280, Norwood, MA 02062. **237**

Circuits

Optical coupler provides ±3 kV or more isolation between output and input. Internal light source is an LED with a drive current of 50 to 100 mA and a cutoff frequency of about 290 kHz. Unit is housed in a standard 14-pin DIP. M7, Inc., 210 Campus Dr., Arlington Heights, IL 60004. **238**

Temperature-compensated oscillator generates frequencies from 3 to 10 MHz. Power consumption for the 1.5- by 1.5- by 0.8-inch unit is <120 mW. Unit price in quantities of 1000 is $42.50. CTS Knights, Inc., Sandwich, IL 60548. **239**

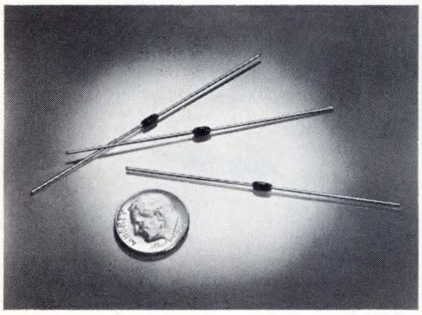
Audio filters, Series 7000, are active/octave bandpass type and have narrow skirts, a flat response, steep attenuation slopes and high rejection out of the pass band. The units are epoxy encapsulated and designed for PC board mounting. Prices for one to four pieces are $240 to $350. Polyphase Instrument Co., E. 4th St., Bridgeport, PA 19401. **240**

High-voltage power supplies, Series AUC, feature adjustable output from −50 to 10% of nominal in 10% steps. Two models cover 1 to 5.5 kV at a nominal 10 mA, and the output is floating. Quantity prices start at $35 each. High Voltage Co., Inc., Northridge, CA 91324. **241**

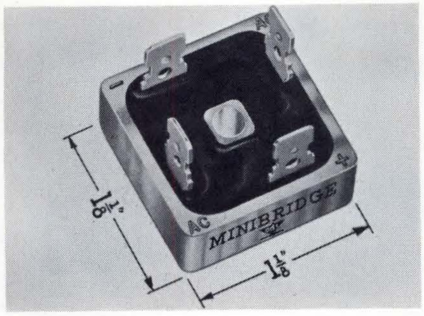
AC line regulators, PEC Series, attenuate low-frequency (below 1 MHz) line noise and transients over 50 dB in OEM applications. Units are rated from 60 VA to 1 kVA and come in 60- or 400-HZ versions. The 60W unit measures 9 by 4.25 by 4 inches and weighs 9 lb. Wanlass, Div. of AMBAC Industries, 525 Virginia Dr., Fort Washington, PA 19034. **242**

DC-to-dc converters, D Series, provide continuous operation over an input range of 18 to 56V dc. Eighteen models are available with 5, 6.3, 12, 15, 24 and 28V dc outputs. Prices range from $155 for 25W to $225 for 100W units. Aaron-Davis Power Conversion Systems, 1150 S. Beverly Dr., Los Angeles, CA 90035. **243**

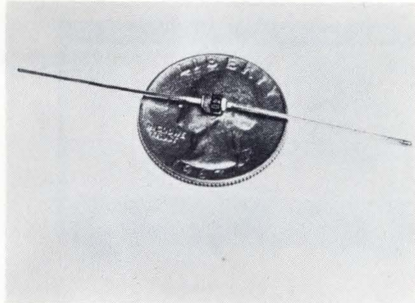
A/D converter, Model 1010, is a bipolar 4-1/2-digit unit that achieves 0.015% accuracy operating with a single input. Conversion speed is 40 msec. A selection of four input voltage ranges and four output code formats is available. Unit price is $255 in 1 to 10 quantities. Libra Systems, Box 161, Collegeville, PA 19426. **244**



Silicon voltage regulator zeners with low dynamic impedance and low bias current requirements are presently being produced with a nominal voltage of 30 to 120V for 1, 3 and 5W applications. The zeners exceed military and aerospace specifications, and are of noncavity monolithic construction with a fused metal hermetic seal. Semtech Corp., 652 Mitchell Rd., Newbury Park, CA 91320. **245**

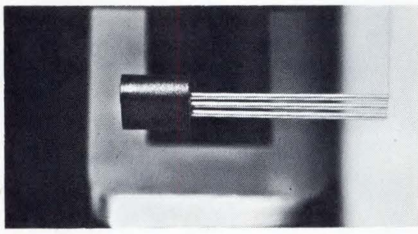


Silicon bridge rectifiers, called "Minibridges," are approximately 1.125 $inch^2$ by 7/16 inch high with 0.193-inch-diam centers for convenient mounting to a heat sink. Rectifiers feature beam lead construction. Universal 3-way terminals make wiring and mounting easier. Typical of these rectifiers is the PA05 rated at 8A and 50 PIV. Electronic Devices, Inc. 21 Gray Oaks Ave., Yonkers, NY 10710. **248**

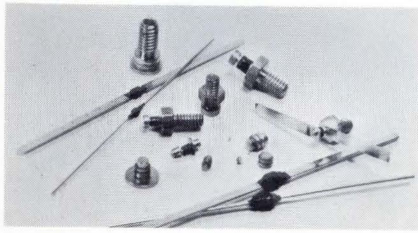


Newly qualified silicon rectifiers, JAN and JAN TX 1N4245 through JAN and JAN TX 1N4249, are available in monolithic glass packages and are totally unaffected by severe moisture or temperature conditions. Compact packages offer weight and space savings for high-density designs. Sensitron Semiconductor, Div. of R.S.M. Electron Power Inc., 221 W. Industry Ct., Deer Park, NY 11729. **251**

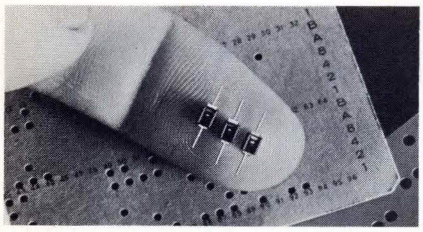
High voltage planar power transistors, the 700V SDT 500 Series, are packaged in JEDEC TO-3 case and are 100% planar construction. Hi-rel mounting (gold-plated molybdenum pedestal) and low leakage levels at elevated temperatures (10 μA at 150°C, 400V_{CEX}) are features of this series. These devices have multiple gain ranges with beta from 40 to 120, 1 to 5A and all are SiO_2 passivated. Solitron Devices, Inc., 1177 Blue Heron Blvd., Riviera Beach, FL 33404. **246**



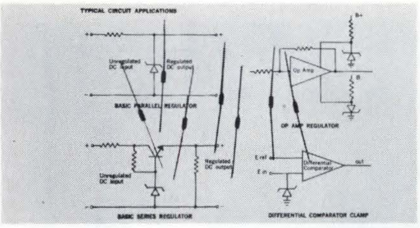
Plastic PUTs, Types P13T1 and P13T2, are functionally equivalent to standard UJTs and provide the added advantage of versatile programming. The latter enables the designer to add external resistors to meet his needs in programming Eta, R_{BB}, I_p and I_V functions. Packaged in a TO-92 plastic case, the devices are fully planar passivated. Prices are as low as $0.55 in 1000 quantities. Unitrode Corp., 37 Newbury St., Boston, MA 02116. **249**



Microwave PIN diodes feature low insertion loss and second and third harmonic levels of 90 dB below fundamental and intermodulation products as low as 60 dB. Applications for PIN diodes include TR switches, duplexers and commercial two-way communications systems. They are also widely used in AGC loops and tumble filters in CATV systems. Cost of these diodes ranges as low as $0.90 in large quantities. Unitrode Corp., 37 Newbury St., Boston, MA 02116. **252**

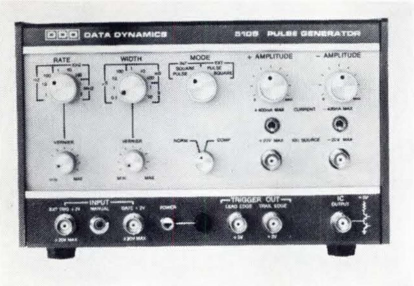


High output phototransistors, STPT-260P "Opto-Paks," mount on 0.087-inch centers for high-speed punched tape or 96-column, 80-column and standard punched card reading. Packaged in a plastic housing measuring 0.085 by 0.105 by 0.045 inch, the device provides an output of 2 mA at 1 mW/cm^2, switches at 6 μsec speed and has a peak spectral response of 800 nm, typical. Sensor Technology, Inc., 7118 Gerald Ave., Van Nuys, CA 91406. **247**

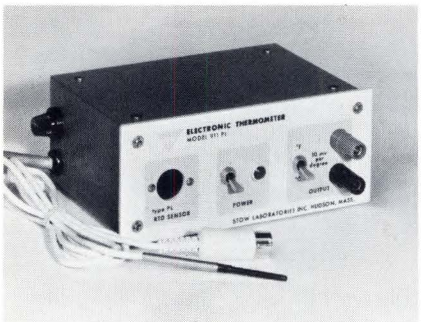


Ultralow-noise low-voltage avalanche zeners, the "LNA" Series, are available with voltages ranging from 2.8 to 10V. Built with extremely sharp knee and tight leakage specifications, they operate at low current levels. Standard devices come in hermetically sealed DO-7 packages and can be supplied in much smaller micro-epoxy package if desired. CODI Semiconductor, Div. of Computer Diode Corp., Pollitt Dr. S., Fair Lawn, N J 07410. **250**

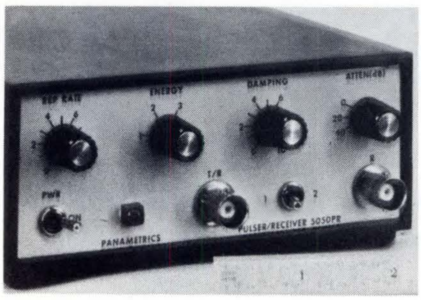
Dual power driver MCH 2890 permits driving of high-current loads directly from logic level devices. This new device translates logic voltage levels to high power outputs. Inputs can be DTL or TTL and loads can be either resistive or inductive. Applications requiring high current pulses that are digitally controlled can now be interfaced with a single package. Motorola Semiconductor Products Inc., Box 20912, Phoenix, AZ 85036. **253**



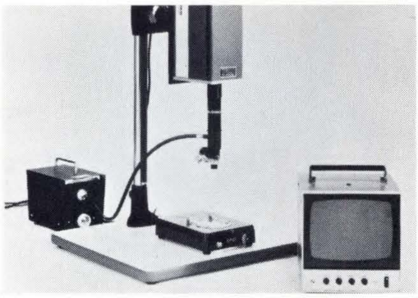
Five MHz pulse generator with 20V output is priced at $300. Model 5105 covers from 0.1 Hz to 5 MHz and provides three simultaneous pulse outputs: positive, negative and current sinking 4.5V. Other features include 100% duty cycle, pulse or square wave output and pulse widths from 10 nsec to 10 sec. Data Dynamics Div., 240 Humphrey St., Englewood, N J 07631. **254**



Electronic thermometer features platinum sensing element, no adjustments and fully interchangeable factory-calibrated sensors and electronics. Output is 10 mV/° for use with digital voltmeters, recorders and loggers. Temperature range is −60 to 200°C with ±0.05°C repeatability. Prices for the Model 911 start at $195 each (including sensor). Stow Laboratories, Inc., 110 Kane Industrial Dr., Hudson, MA 01749. **255**

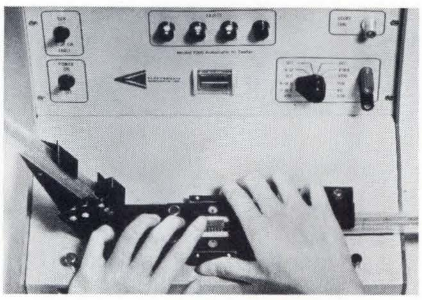


Ultrasonic pulser-receiver, Model 5050PR, is a broadband, high-resolution ultrasonic instrument that covers the frequency range from 0.1 to 30 MHz. It is used with an oscilloscope and ultrasonic transducers. Panametrics, Subs. of Esterline Corp., 221 Crescent St., Waltham, MA 02154. **256**



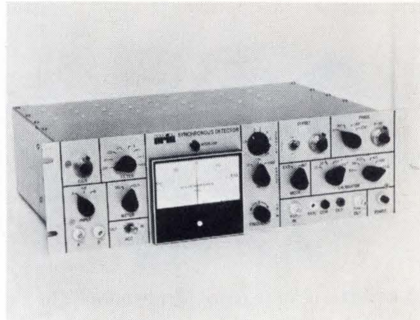
Television-microscope system, Model MV 9000, is a fully coordinated CCTV system for microscopic examination up to 600 power. It includes a high-resolution camera, a solid-state monitor, complete optical system, adjustable camera platform and a fiber-optic illumination system. Circon Corp., Santa Barbara Airport, Goleta, CA 93017. **257**

"Data recording and transmission terminal in a briefcase", Model 2002, has full alphanumeric capability, a strip printer and (an option) provides two way communication with EDP center. A cassette recorder, the communications module and a rapid recharger for the nickel cadmium battery are fitted into the briefcase. Both recorder and keyboard can be removed for desk-top operation. MSI Data Corp., 1381 Fischer Ave., Costa Mesa, CA 92627. **258**

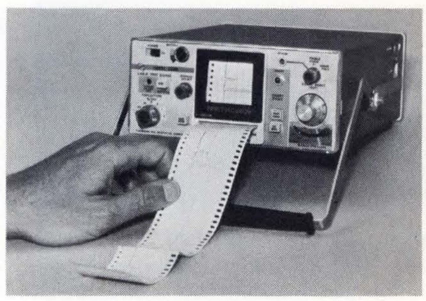


IC test system combines an automatic digital IC tester with a semi-automatic handler. Designed for small- to medium-quantity users, the system uses shipping tubes for both input and output containers. Price is less than $2000. Electrodata Concepts, Inc., 69 Connecticut Ave., Norwalk, CT 06854. **259**

Portable photometer priced at $295 each is available with a selection of four different probes with sensitivity to 0.0002 footcandles. Features of the Model 3100 include sensitivity from 0.001 to 10,000 footcandles, 5% full-scale accuracy, 3% linearity and a recorder output of 1V to 1 mA. Vactec, Inc., 2423 Northline Industrial Blvd., Maryland, MO 63043. **260**



Phase sensitive detector features a digitally derived square-wave reference oscillator output with a linear phase adjustment control. Model ESE3000 has its oscillator and amplifier-detector units completely decoupled and isolated from chassis ground. Frequency range is 10 Hz to 10 kHz with 100 kΩ/50 pF input impedance. Price each is $2660. Advanced Research Instrument Systems, Inc., 6500 Tracor Lane, Austin, TX 78721. **261**



Portable TDR, Model 1501, has a plug-in recorder that permits high resolution recordings at the touch of a button. Its X-Y output is suitable for most oscilloscopes. Step pulse risetime is 1.3 nsec and amplitude is 1V on battery and 10V on ac power. Price is $1900. Tektronix, Inc., Box 500, Beaverton, OR 97005. **262**

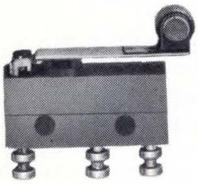
NEW

smallest precision snap action switch yet!

Case dimensions of our new 4900 Series MINI-MITE switches are less than .250″ by .300″ by .100″. Ratings are 2 amp. 125-250V AC; 2 amp. (Res.) and 1 amp. (Ind.), 30V DC. Meet MIL-S-8805 specs. Available with 4 types of terminals, pin plunger and various lever type actuators.

new sub-miniature switches

Our new 4800 Series sub-miniature switches are rated 5 amp. 125-250V AC with 5 amp. resistive and 2½ amp. inductive ratings at 30V DC. Case dimensions are approximately .400″ by .800″ by .250″. Available with 6 terminal types, a variety of lever actuators and optional bifurcated or dual gold contacts. Meet MIL-S-8805 specs. McGill Manufacturing Co., Inc., Electrical Division, Valparaiso, Indiana 46383



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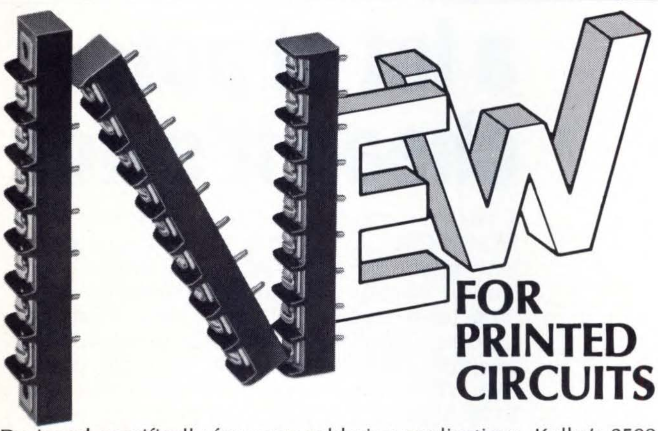

FOR PRINTED CIRCUITS

Designed specifically for wave-soldering applications, Kulka's 2500 and 2600 Series feature rotation resistant terminal pins in widths of .062 or .093 to fit standard printed circuit board holes. Rated at 20 AMPS, 1100 VOLTS RMS the Series is available in a vairety of molded materials, terminations and surface hardware including Kulka's quick-connect Kliptite™ terminals.
Specifications and ordering information are listed in Kulka's Printed Circuit Terminal Board Catalog. Send for a copy today.
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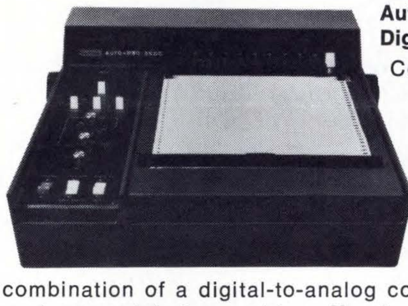
CIRCLE NO. 57

Beckman simplifies time-sharing, data acquisition and display.

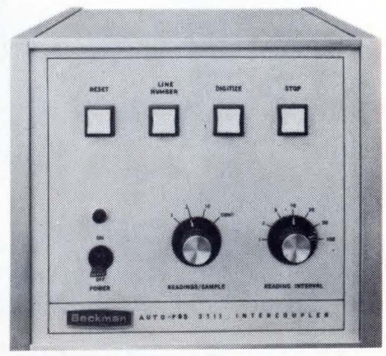


Auto-Pro 3500 Digital Plotter

Costing about $1000 less than most other plotters and designed for the scientific user, the AP-3500 is simple to use with either time-share or small computers. The combination of a digital-to-analog converter Y axis and an incremental stepper-driven X axis removes paper size restrictions and affords complete capability for 90% of all plotting/recording applications. The AP-3500 displays computer-calculated digital data or analog information directly. As a time-share plotter, information is accepted serially in ASCII arrangement at either standard or high-speed rates; as a minicomputer peripheral, data is accepted in bit parallel form, permitting even higher plotting speeds.

Plotting is in continuous form — forward or reverse — on roll chart paper, with only one data word and control character required to uniquely position the pen. Usable with modern high-speed data terminals, the AP-3500 plotter has overall accuracy of better than ±0.25% and is an ideal analytical tool in most scientific applications, ranging from biochemistry to circuit design. Request Bulletin AP-2402 for complete details.

Auto-Pro Intercouplers



Designed as a complete data system, Beckman's AP-3111 Intercoupler takes an analog input, converts the information to digital form, then prints and punches the data on an ASR-33 teletypewriter. Companion unit to the AP-3111 is Beckman's Auto-Pro 3109 which accepts up to 16 BCD data bits in place of the analog input. Paper tape outputs of both instruments are directly time-share compatible and include automatic line number update and special control characters. Other features are local or remote control; preselectable reading interval and number of readings per sample. Request Bulletins AP-2400 and AP-2401 for complete details.

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CIRCLE NO. 58

Pulse laboratory amplifier, Model 4313-P, has typical risetime of 1 nsec at $\pm$6V into 50Ω. Droop is less than 1% at 100 nsec, and typical linear output is $\pm$6.5V. Dynamic range is greater than 70 dB at all gain settings. Prices begin at $1195. C-COR Electronics, Inc., 60 Decibel Rd., State College, PA 16801. **263**

Circuit verifier, the "Auto/Scan 200," is a low-cost, high-speed, automatic, fixed-sequence circuit verifier. Training is minimized by point-to-point stepping and simple controls. Everett/Charles, Inc., 2806 Metropolitan Pl., Pomona, CA 91767. **264**

TV cameras give a usable picture with only 0.003-footcandle illumination on the image tube. They can be aimed directly at the sun without damaging the silicon-diode-array vidicon. Model 4250 for severe environments and Model 4350 for normal environments give horizontal center resolution of 650 lines with 350 lines vertical center. Cohu Electronics, Inc., Box 623, San Diego, CA 92112. **265**

Programmable system for checking continuity and short circuits is expandable up to 10,000 wires or connections in modules of 50. Prices start below $3000, and expansion costs less than $10/channel. A. D. Automation, 830 Linden Ave., Rochester, NY 14625. **266**

Thermally controlled platforms for chip, wafer and hybrid circuit testing provide accuracy $\pm$1°C and stability of $\pm$0.3°C. Model TP3003 is an accessory to the TP2000 ThermoSpot and covers the -30 to 95°C range. Temptronix Inc., 591 Hillside Ave., Needham, MA 02194. **267**

PLO/synthesizer is a data processing unit for extremely precise timing or frequency measurements in signal analysis of magnetic tape recordings. Model I-1001 has tuning range from 1 to 20 MHz and can accept any reference frequency off the tape in the range between 100 Hz and 20 MHz. Price is $5850. Probe Systems Inc., 655 N. Pastoria, Sunnyvale, CA 94086. **268**

Acoustic monitor, Model AR-2, continuously records the peak sound levels of noise. Ranges available include 50-90, 70-110, 90-130 and 110-150 dB. Features include linear scale, battery power and portability. Dallas Instruments, Inc., Box 38189, Dallas, TX 75238. **269**

One-kilowatt amplifier is flat from 10 kHz to 220 MHz. Model M406L has 60-dB power gain with flatness of better than $\pm$1.5 dB. Rise and fall times are 7 nsec. Price with all options is $22,000. Instruments For Industry, Inc., 151 Toledo St., Farmingdale, NY 11735. **270**

DC instrumentation amplifier, the wide-band differential Model 117, amplifies signals from floating or grounded low-level transducers and supplies 10V output at 100 mA. Specifications include gains to 1000, bandwidth from dc to 100 KHz, CMR of 100 dB at 10V and drift less than 5 μV/°C. Price is $350. Incor Instrumentation, Inc., 29 Newton Rd., Plainview, NY 11803. **271**

Paper winder for teleprinters, Model 2012, mounts directly on a Model 28 or 35 Teletypewriter in minutes. Adapter plates are available for mounting to other teleprinters such as Model 33. Single unit price is \$74.50. Logic Systems Corp., 1567 Cypress Dr., Jupiter, FL 33458. **272**

Charge amplifiers for all piezoelectric sensors are priced at only \$79.95. Model 4101 has dynamic measuring capability of better than ±1 to ±10,000 pcmbs at the input. It can be used with over 1000 ft of cable. Columbia Research Laboratories, Inc., MacDade Blvd. & Bullens Lane, Woodlyn, PA 19094. **275**

Measuring microphotometer has accuracy of 0.001 mm over a 254-mm range. Optional printout equipment includes punch paper tape, line printers, mag tape and a time-sharing terminal interface. System price is less than \$20,000. Rank Precision Industries, Inc., 411 E. Jarvis Ave., Des Plaines, IL 60018. **278**

Strain gage simulator (decade resistor), Model 40, has steps of 0.01, 0.1, 1.0, 10 and 100Ω each and features ±0.02% accuracy of setting. Price is \$225. Vishay Instruments, Inc., 63 Lincoln Hwy., Malvern, PA 19355. **273**

Resistance bridge module covers seven decades and has 5 PPM accuracy. Model 1104 has a resistance range from 1Ω to 1 MΩ using a Kelvin bridge. Price is \$1275. Vishay Resistor Products, 63 Lincoln Highway, Malvern, PA 19355. **276**

Real-time programmer permits accurate control of 25 functions for up to 1 week in advance. Model 5025 time gate features accuracy of ±2 sec/year and can also serve as a master clock. Broadcast Products, Inc., 660 Lofstrand Lane, Rockville, MD 20850. **279**

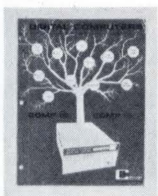
Laboratory differential amplifier, Model 4333, has both a 400 V/μsec slew rate and 3-dB bandwidth of dc to 20 MHz. The unit is designed for both CW and pulse use. Options include differential or single ended input, gain of 26 or 20 dB and various impedances. Prices for this half-rack-size instrument start at \$650. C-COR Electronics, Inc., 60 Decibel Rd., State College, PA 16801. **274**

Temperature recorders are inkless, available for various temperature spans between 0 and 2000°F and 0 and 1000°C and offered with chart speeds from 1/8 inch to 480 inches/hr. There are models for both iron-constantan Type J and chromel-alumel Type K thermocouples. Price, without thermocouple, is \$130. Omega Engineering Inc., Box 4047, Stamford, CT 06907. **277**

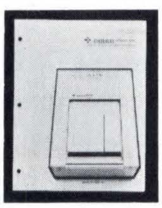
Bit error rate tester, Model 2350 "Bert," furnishes pattern choices of 1:1 (reversals) plus a choice of 63, 511 and 2047-bit pseudorandom test patterns for test and evaluation of modems and data/telegraph transmission systems. Internal crystal-controlled clock speeds from 50 to 2400 baud are provided. Digitech Data Industries, Inc., 66 Grove St., Ridgefield, CT 06877. **280**

"Programming Systems" is a 41-page catalog that describes various patchboard programming systems. A product description section provides specifications and dimensional information. Patchcords and accessories are also included. Virginia Panel Corp., Box 1106, Waynesboro, VA 22980. **281**

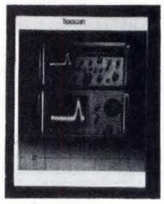
Stepping motors are covered in Catalog P-431. Four motor models and two translator cards are described with specifications, diagrams and dimensional data. Warner Electric Brake & Clutch Co., 449 Gardner St., Beloit, WI 53511. **282**



Digital computer brochure describes the COMP-16 and COMP-18 minicomputers and peripheral equipment. The fast Fourier-transform processor is also featured in this 16-page brochure which includes illustrations, specifications and engineering drawings. UniComp, Inc., 18219 Parthenia St., Northridge, CA 91324. **283**



Multichannel recorder with up to four 40mm-wide channels is described in Bulletin 934-19. This four-page brochure covers detailed specifications, outline dimensions, ordering information, accessories and supplies and descriptions of compatible signal conditioners. Gould Inc., Instrument Systems Div., 3631 Perkins Ave., Cleveland, OH 44114. **284**

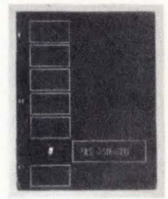


Spectrum analyzers, sweep generators, programmable attenuators and lumped-component miniature lowpass and bandpass filters are described in this 20-page catalog. Physical and electrical characteristics are given along with applications and prices. Texscan Corp., 2446 N. Shadeland Ave., Indianapolis, IN 46219. **285**

Ceramic substrates are covered in Technical Bulletin 712. Information provided includes material descriptions, design information and a list of stock substrates. American Lava Corp., Laurens, SC 29360. **286**

Linear variable differential transformers are discussed in this eight-page catalog. Some applications for LVDTs are given along with a comparison chart of various types of transducers. Measurement and price ranges of typical units are included. Schaevitz Engineering, Box 506, Camden, N J 08101. **287**

Custom-engineered potentiometers including conductive-plastic, wire-wound precision and special potentiometer combinations are described in Brochure CEC-1. Potentiometric pressure transducers and miniature snap-action pressure switches are also included. Amphenol Controls Div., Bunker Ramo Corp., 120 S. Main St., Janesville, WI 53545. **288**



Pulse generator brochure describes a complete line of generators, including plug-in and non plug-in types and a computer controlled pulse generator system. A selection guide allows easy comparison of performance specifications. Hewlett-Packard Co., 1601 California Ave., Palo Alto, CA 94304. **289**

Template catalog lists over 475 types to meet the needs of architects, engineers, designers and draftsmen. A complimentary all-purpose template is also supplied. Alvin & Co., Inc., 609 Palisado Ave., Windsor, CT 06095. **290**

SCR and triac catalog contains complete specifications, case drawings and performance curves of over 300 standard devices, including SCRs from 25 to 800V, 5 to 60A and triacs from 50 to 600V, 1 to 40A. Centralab Distributor Products, 5757 N. Green Bay Ave., Milwaukee, WI 53201. **291**

Digital cassette recorder catalog provides typical applications, advantages of bit-by-bit incremental recording vs continuous buffered incremental recording, fundamental descriptions and specifications for a wide range of continuous and incremental digital cassette recorders. Memodyne Corp., 369 Elliot St., Newton Upper Falls, MA 02164. **292**

Literature

Electronic test equipment is featured in a 48-page catalog that provides specifications and prices for signal generators, Q meters, frequency converters, power supplies, counter-timers, microwave components and other electronic test equipment. Baynton Electronics, 2709 N. Broad St., Philadelphia, PA 19132. **293**

Miniature solid-state electronic buzzer for devices requiring audible signals at low power is described in Bulletin GA100. Projects Unlimited, Inc., 1926 E. Siebenthaler Ave., Dayton, OH 45414. **294**

Connector condensed catalog lists eight different series and provides pertinent specifications. Types included are: printed circuit, removable contacts, center screw lock, rack and panel, power, terminal blocks, test point and special designs. Continental Connector Corp., 34-63 56th St., Woodside, NY 11377. **295**

DIP reed relay Bulletin No. 688 lists 40 versions of the DIP line of 8-pin reed relays. Magnecraft Electric Co., 5575 N. Lynch Ave., Chicago, IL 60630. **296**

Modular optical linear encoders are covered in a two-page product sheet describing the Mod-Coder/L encoders. The brochure lists features and applications and provides a photo and outline drawing. Sequential Information Systems, Inc., 249 N. Saw Mill River Rd., Elmsford, NY 10523. **297**

Solid-state laser, Series 104A, is featured in a 12-page brochure covering more than 40 different ruby, glass and YAG systems and accessories. Included are instructive data on laser principles and applications. Hadron, Inc., 800 Shames Dr., Westbury, NY 11590. **298**

Thumbwheel switches are described in four-page brochure CS901-R1. Specifications, circuit diagrams, truth tables and a complete selection guide are provided. A. W. Haydon Co., 232 N. Elm St., Waterbury, CT 06720. **299**

Thermistor catalog provides a brief introduction to a broad variety of thermistor sensors and sensor assemblies. Included is a description of a variety of thermistor types and an extended line of experimental thermistor kits. Fenwal Electronics Inc., 63 Fountain St., Framingham, MA 01701. **300**

Literature

Closed-cell polyolefin foam, "MACmount 9760," is coated on two sides with a pressure sensitive adhesive. A technical bulletin describes its use for critical fastening, assembling and permanent bonding applications. Morgan Adhesives Co., 4560 Darrow Rd., Stow, OH 44224. **301**

Hermetic high-reliability metallized plastic DIPs for MSI/LSI circuits are detailed in Technical Bulletin No. 175. Performance and costs of this package are compared to ceramic and encapsulated types. A list of standard packages is provided, along with notes on low cost assembly. U.S. Electronic Services Corp., Holgar Industrial Park, Clifton Heights, PA 19018. **302**

Wire, cable and cordset catalog, No. CEC-MC-571, contains 92 pages of product data and includes comparison charts of different types of insulating materials, copper wire specifications, estimating charts and current ratings. Columbia Electronic Cables, 11 Cove St., New Bedford, MA 02744. **303**

Custom-designed dc motors and prong-mounted power supplies are the subjects of a 16-page brochure that lists the entire motor line by horsepower, output rpm and torque according to dimensional and weight requirements. Performance curves for all products and a conversion table for power supplies are included. Rowe Industries, Inc., Bridgehampton Tpke., Sag Harbor, NY 11963. **304**

Semiconductor diode catalog provides detailed information on specifications and dimensions of voltage-variable capacitors, low current zeners and TC reference diodes, logarithmic, high voltage, multi-junction, noise and ultra-low leakage diodes. CODI Semiconductor, Div. of Computer Diode Corp., Pollitt Dr. South, Fair Lawn, N J 07410. **305**

Trimmers, potentiometers and turn-counting dials are featured in short form catalog CSF-2. Specific performance characteristics are provided for wirewound and infinite resolution trimmers, 1-, 3- and 10-turn precision potentiometers and custom-engineered components. Amphenol Controls Div., Bunker Ramo Corp., 120 S. Main St., Janesville, WI 53545. **306**

Silicon bridge rectifier pocket guide provides comparative information on units supplied by various manufacturers. Complete electrical ratings plus outline drawings are included. General Instrument Corp., 600 W. John St., Hicksville, NY 11802. **307**

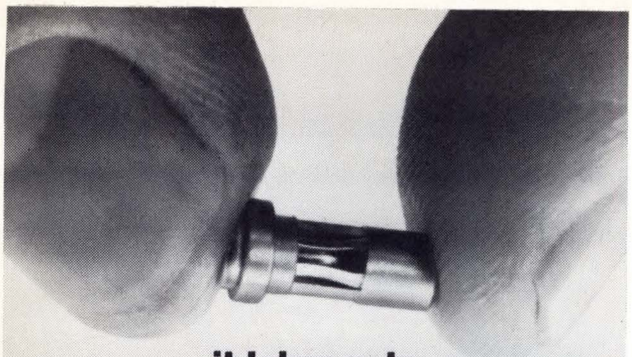
Teflon terminals catalog provides a full listing of all standard terminals types including stand-offs, feed-thrus, metal base, test jacks, test probes and transistor sockets, in miniature, subminiature and microminiature sizes. A schedule of suggested resale prices and quantity discounts is also included. Herman J. Smith Inc., 812 Snediker Ave, Brooklyn, NY 11207. **308**

Absolute shaft encoders for industrial and scientific applications are described in Bulletin 67-21A. Specifications, physical details and options are given for the encoders which feature three to six digits of range in several codes. Theta Instrument Corp., Fairfield, N J 07006. **309**

Silicon resistors with positive temperature coefficient are described in Data Sheet CP 5-1-71. Construction features are illustrated, and environmental performance is presented in a table. Resistance vs temperature curves are provided for 40 standard resistor values. Ward Leonard-Hagerstown Div., Angstrohm Precision, Inc., Box 1827, Hagerstown, MD 21740. **310**

Automatic range expander that enables strip chart recorders connected to laboratory instruments to record off-scale data without attenuating or decreasing instrument sensitivity is described in a data sheet with specifications and applications. Cahn Instruments Div., Ventron Corp., 7500 Jefferson St., Paramount, CA 90723. **311**

Test equipment for electronic servicing, school, laboratory and industrial applications is featured in Catalog BK2. This 24-page catalog encompasses a wide range of equipment from a 100% mutual-conductance tube tester to a dc to 100 MHz triggered sweep oscilloscope. Dynascan Corp., 1801 W. Belle Plaine Ave., Chicago, IL 60613. **312**



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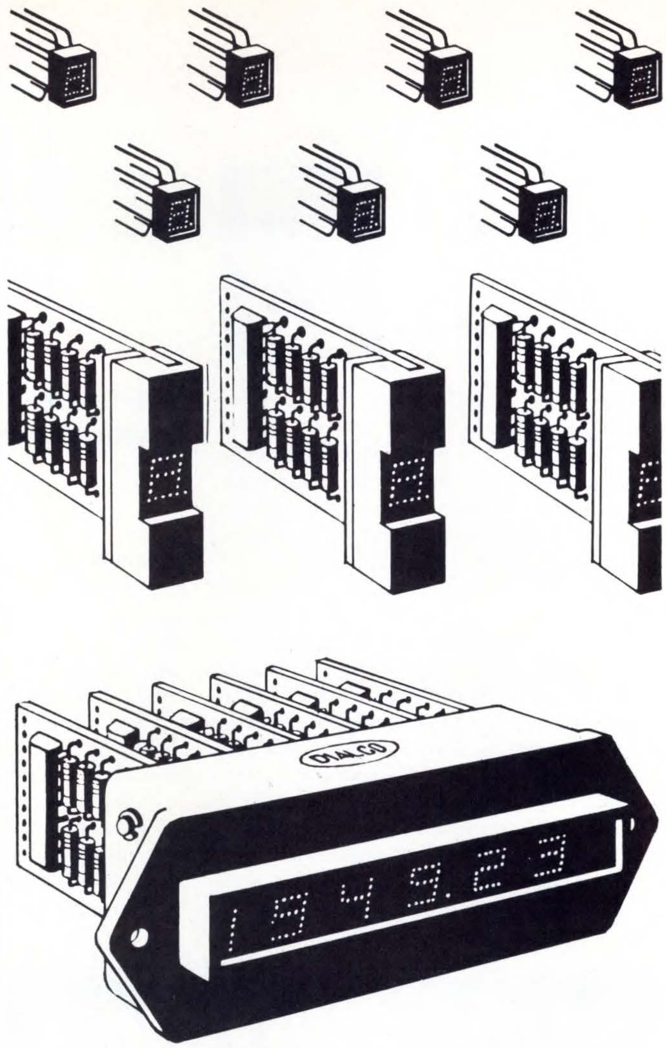
CIRCLE NO. 65



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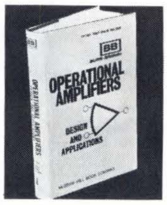
CIRCLE NO. 73

Operational Amplifiers —Design and Applications



Burr-Brown; McGraw-Hill; 1971; Over 500 pages; $15.00.

Written by the applications and engineering staffs of Burr-Brown, this book presents a complete treatment of the design and application, as well as the theory and testing, of operational amplifiers.

To treat the major aspects of op amp technology, the book is divided into two parts and two appendices. Part 1 considers the design of op amps, discusses factors which determine performance characteristics and outlines the techniques available for their control. Part 2 presents practical op amp applications. Appendix A reviews basic theory of op amps, and appendix B gives definitions of performance parameters used to characterize them and provides associated test circuits. Order with check or money order payable to Burr-Brown Research Corp., International Airport Industrial Park, Tucson, AZ 85706. Outside of U.S. and Canada add $1.80 postage.

"Printed Wiring Design Guide"

A manual for users and designers of rigid and flexible interconnection printed wiring structures. It is divided into 10 major sections covering such topics as: design considerations; fabrication information; single-sided and double-sided rigid printed wiring boards; rigid multilayer boards; flexible printed wiring; considerations for mounting circuit components and mechanical parts; documentation; testing; and information on the state-of-the-art concerning computerized techniques used to assist in the design of printed wiring. Price is $100 which includes all additional information for one year. Buyers have the option of having their guides maintained at an annual cost of $25. Institute of Printed Circuits, 1717 Howard St., Evanston, IL 60202.

Also Worth Noting

"Environmental Science—Challenge for the Seventies" is the third annual report of the National Science Board. The report, which examines the present status of environmental science, concludes that "Environmental science today is unable to match the needs of society for definitive information, predictive capability and the analysis of environmental systems as systems." To meet this crisis, the report recommends a course of action in terms of a national program, priorities, organization and manpower. Copies are available from the Superintendent of Documents, U.S. Government Printing Office, Washington, D C for $0.40 per copy.

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Application Notes

"High-Frequency Transistor Primer" is designed to familiarize the microwave designer with terminology used in describing the characteristics of high-frequency transistors. It also discusses the capabilities and limitations of these devices. Avantek, Inc., 2981 Copper Rd., Santa Clara, CA 95051. **315**

"Advantages of Dual-Metal Components in a Miniature Interconnection System" is an eight-page note illustrated with diagrams, graphs and microphotographs to compare dual-metal and single alloy construction techniques in connector design. Berg Electronics, Inc., New Cumberland, PA 17070. **316**

"Solvent Compatibility and Electronic Cleaning" is a four-page technical report describing the properties that determine the compatibility of electronic grade solvent cleaners with electronic components and the parameters to follow in selecting an appropriate solvent. Alpha Metals, Inc., 56 Water St., Jersey City, N J 07304. **317**

Monolithic IC audio amplifier that is short-circuit protected is described in a specification and application report illustrated with circuit diagrams, performance curves and recommended PC layouts for various applications. Plessey Electronics Corp., 170 Finn Ct., Farmingdale, NY 11735. **318**

Dielectric properties of Teflon TFE and FEP resins for microwave engineers is detailed in a 17-page booklet with numerous graphs containing electrical and electronic design data. Du Pont Co., 1542 Farmers Bank Building, Wilmington, DE 19898. **319**

Power voltage regulators are the subject of a 16-page application bulletin that discusses circuit arrangements providing excellent stability vs temperature, load and input voltage variation. Performance curves for several monolithic regulators are included. European Electronic Products Corp., 10180 W. Jefferson Blvd., Culver City, CA 90230. **320**

"Audio-Video Phase Meter with High Sensitivity and High Accuracy" is an article that discusses the operation of phase meters of the zero-crossing detection type together with some of their capabilities. It is featured in Vol. 2, No. 1 of *Technical Review*. Wiltron Co., 930 E. Meadow Dr., Palo Alto, CA 94303. **321**

"Thermoelectric Handbook" contains background history of the theory and development of the Peltier and Seebeck effects along with their applications in electronics, medicine and research. Cambridge Thermionic Corp., 445 Concord Ave., Cambridge, MA 02138. **322**

Electrically-conductive epoxy is compared with eutectic chip bonding in a 20-page test report. Mechanical and electrical tests were conducted on several types of epoxy bonds after they underwent environmental stress. The report is available by writing on company letterhead to Epoxy Technology, Inc., 65 Grove St., Watertown, MA 02172.

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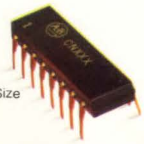

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